I³N Innovative Integrated Instrumentation for Nanoscience

polifab POLITECNICO DI MILANO

POLITECNICO MILANO 1863

Seminar within the “Quantum Circuits and Devices” course

Measuring quantum devices below 4K

Cryogenic electronics

Giorgio Ferrari

Milano, December 2023

Who I am

Innovative Integrated Instruments for the Nanoscience Lab

M. Sampietro G. Ferrari
D. Natali F. Zanetto
+ E. Prati (UniMI)

Photonic Integrated Circuits
Control electronics for large-scale programmable photonic circuits (telecom, sensing, optical computing…)

Quantum computing
Cryogenic electronics for the readout and characterization of spin-based qubits

Biosensors and bio-inspired electronics
Electronic sensors for virus, antibodies, DNA

CMOS neuromorphic circuits for ultra-low power data acquisition and processing

POLIFAB – Clean room facility

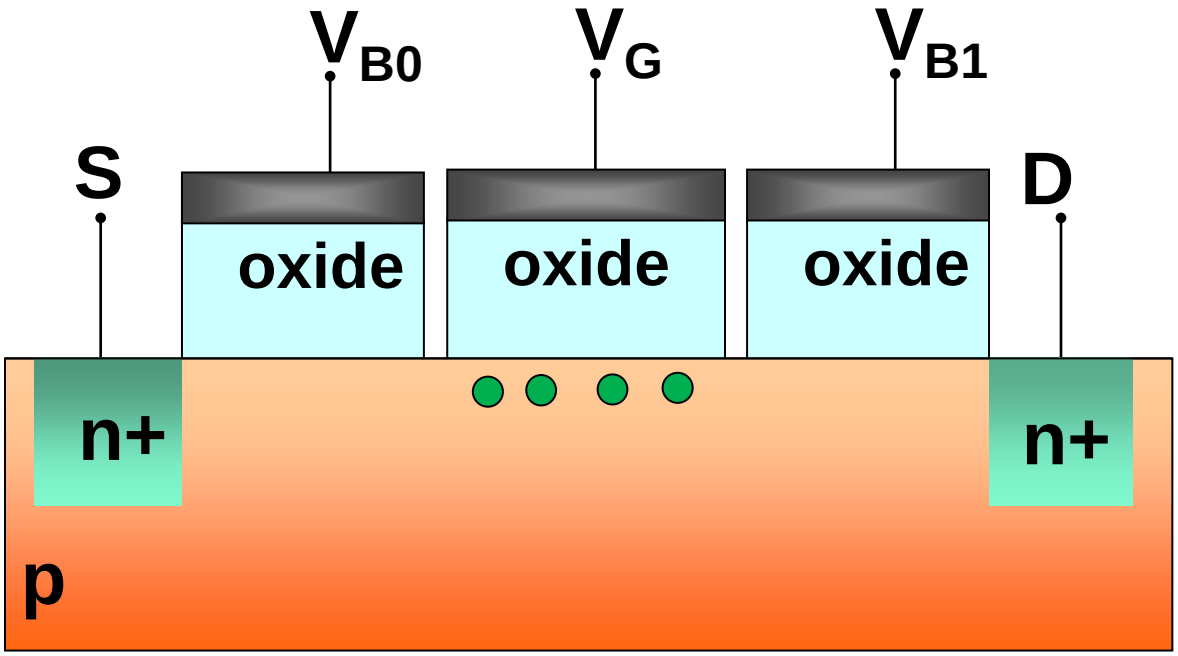
Cleanroom surrounded by a cluster of labs of micro- and nanoelectronics, photonics, photovoltaics, biotechnologies, spintronics, organic semiconductors

I3N lab is part of **polifab**, the micro and nano technology center of the Politecnico di Milano (750 m^2 of clean room)

Outline

- Spin detection using room temperature instrumentation
- Cryogenic electronics
  - Challenges
  - Design rules
- Examples & state of the art

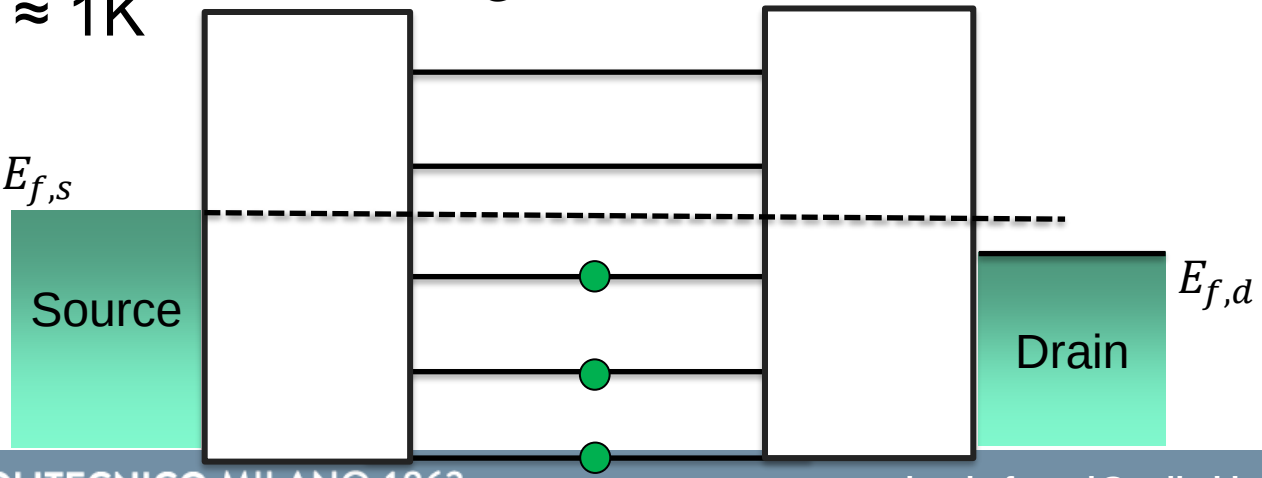
Single-Electron Transistor (SET)

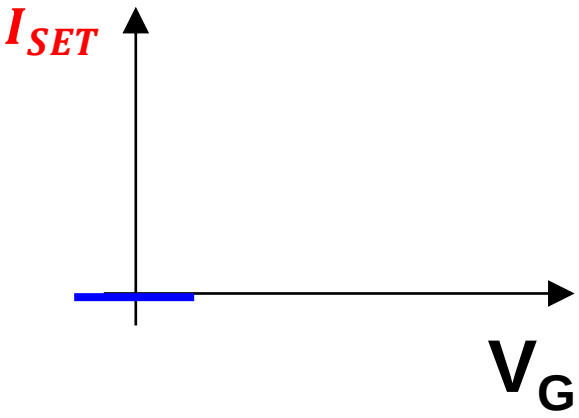


V_{B0}, V_{B1} biased to have an energy barrier for the electrons
The energy barrier is thin enough to allow tunneling

V_G controls the energy levels of the island

T ≈ 1K





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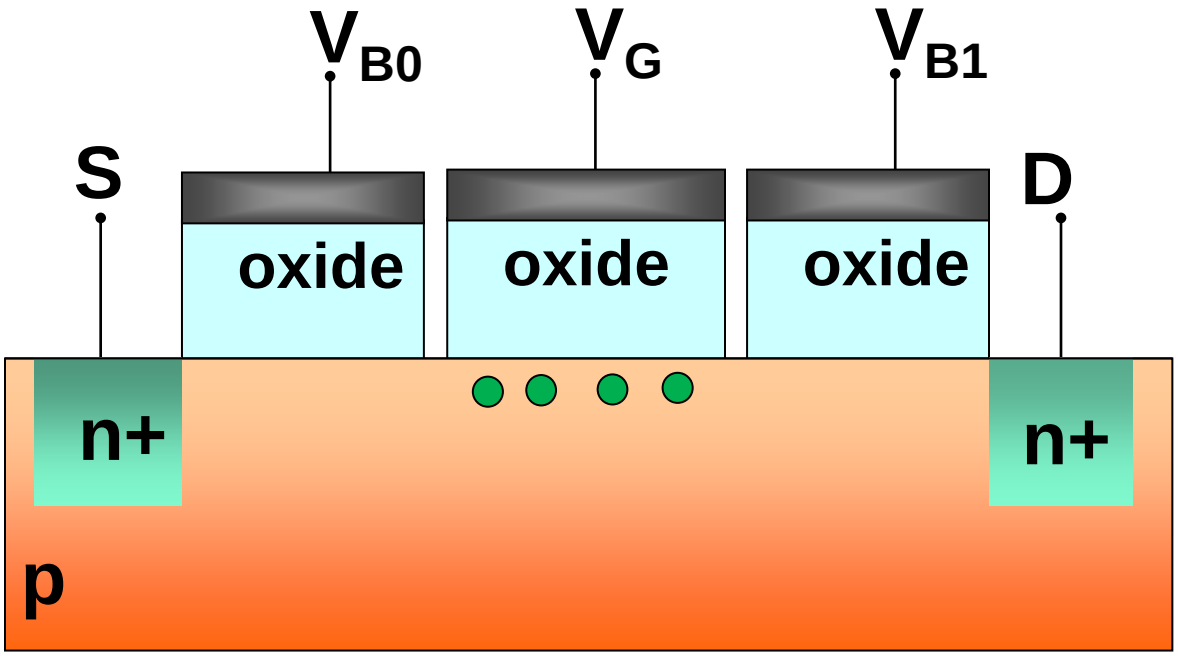

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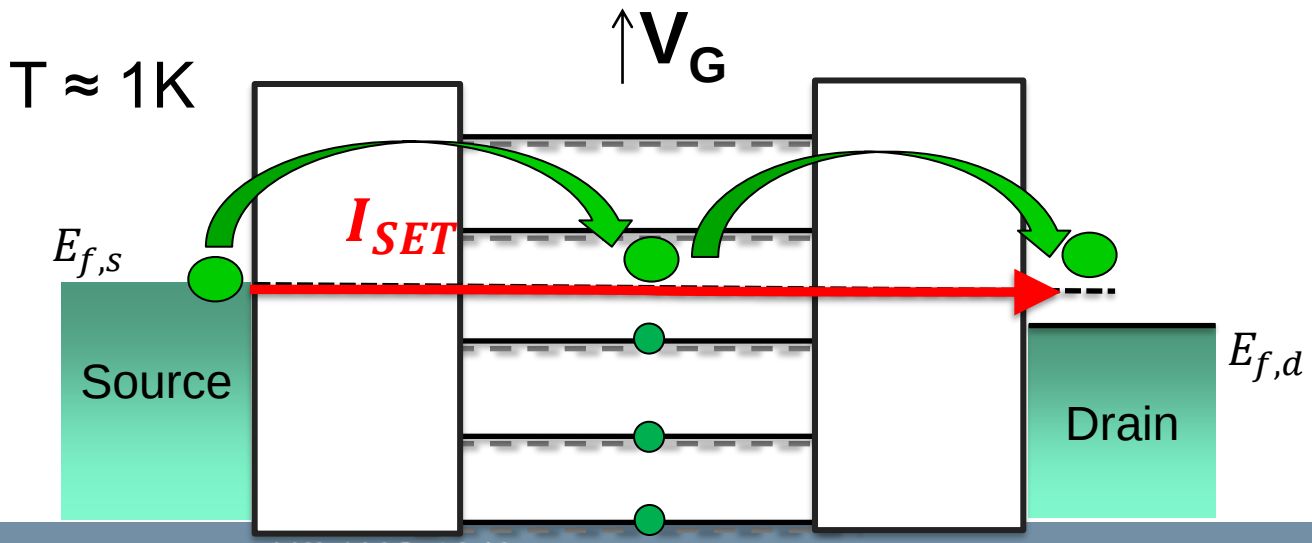

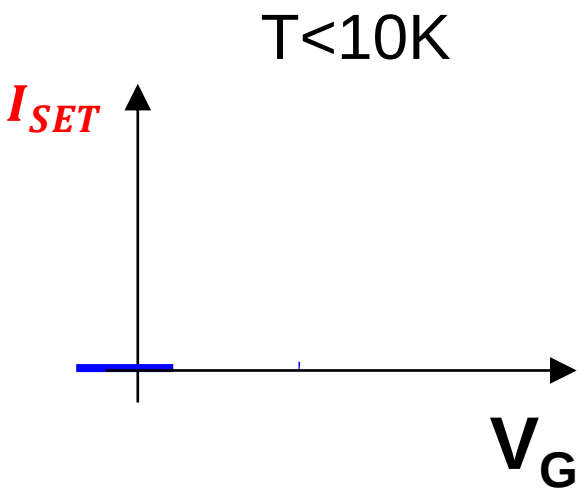

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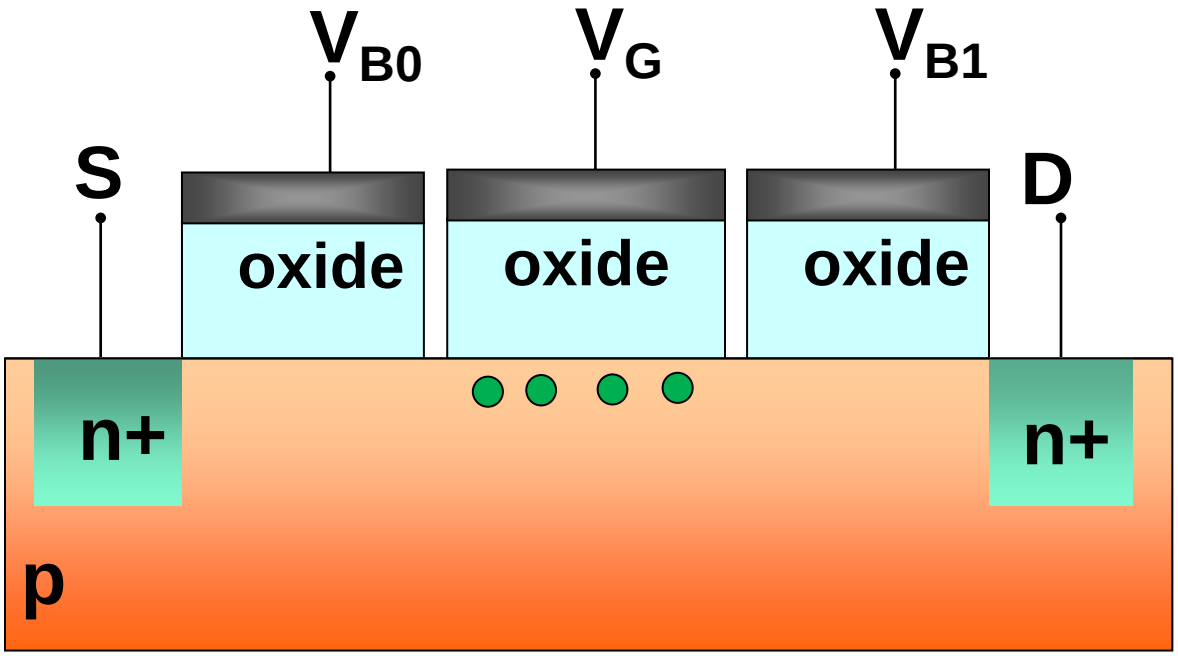

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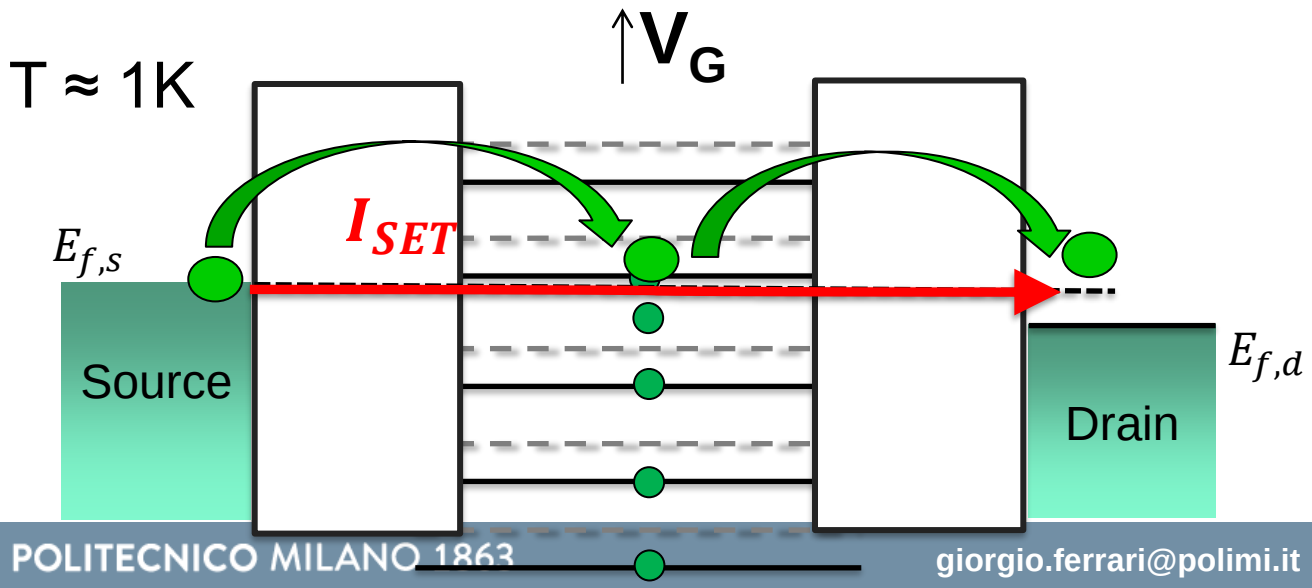
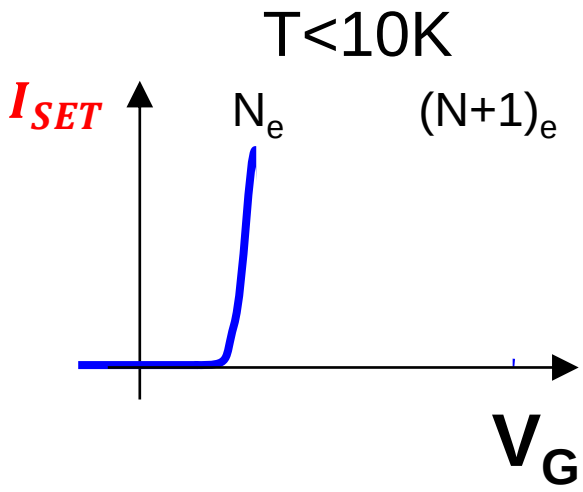
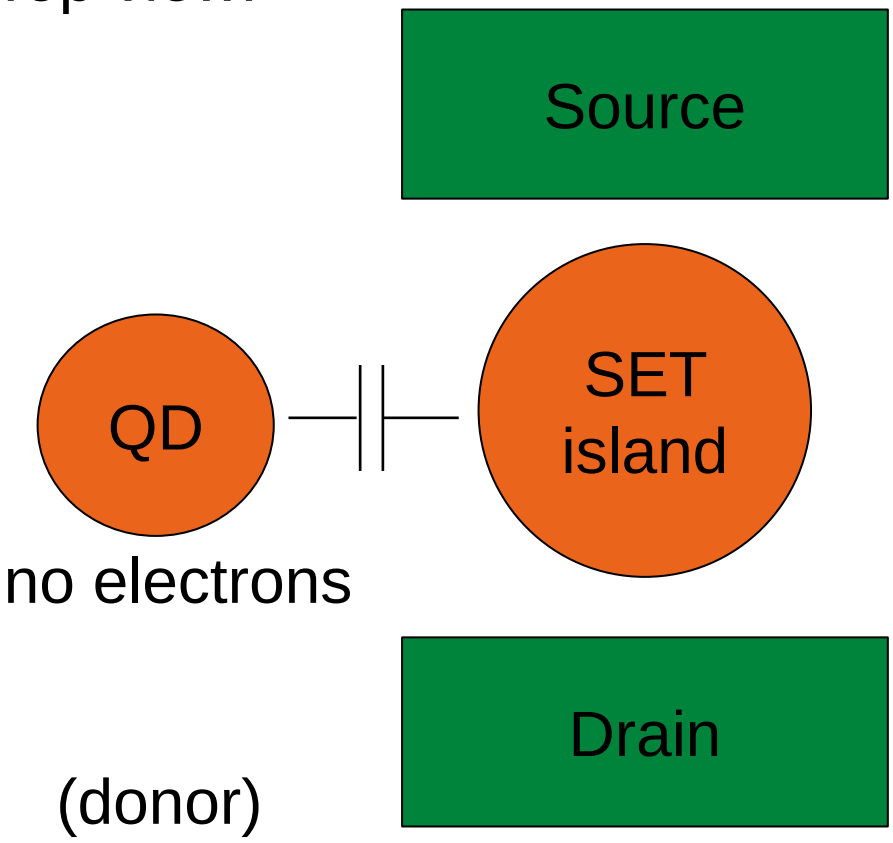


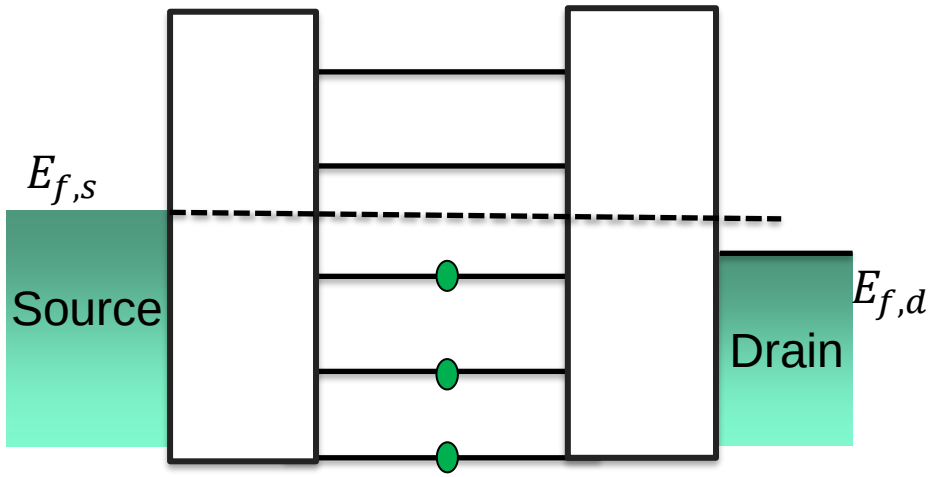


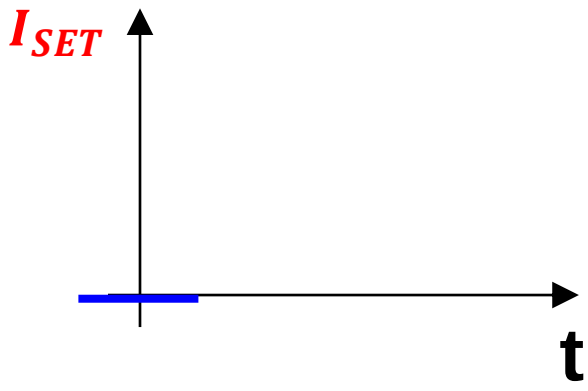
SET-based single-charge detector

Top view:



Energy levels:





SET-based single-charge detector

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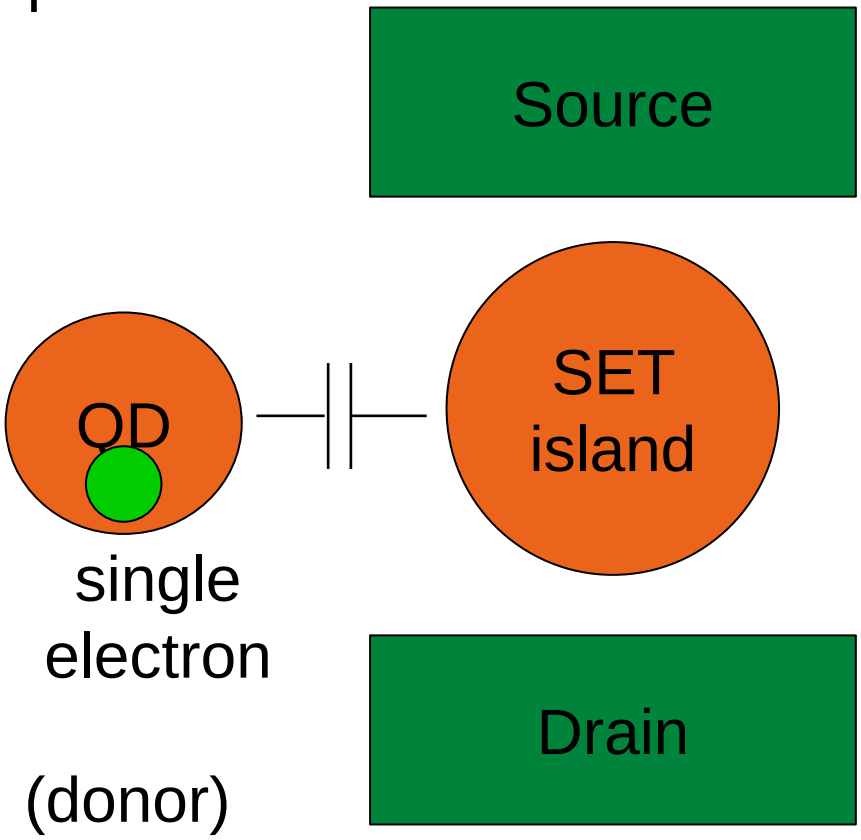

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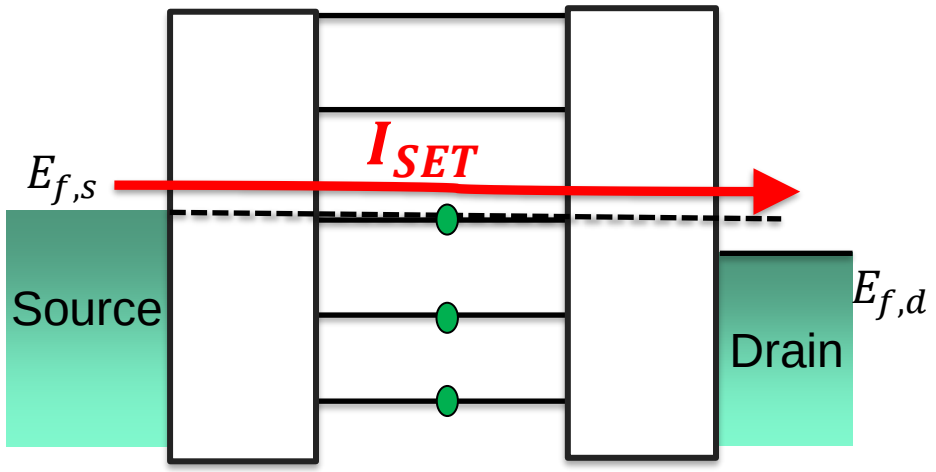
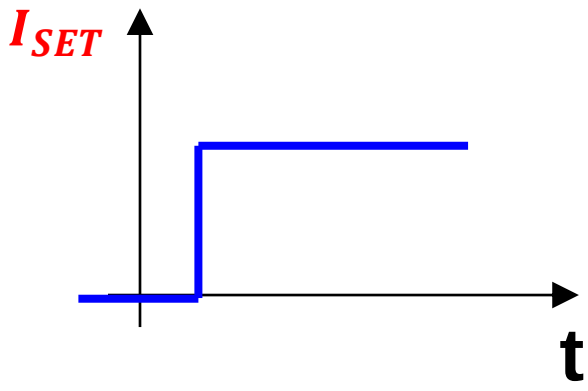
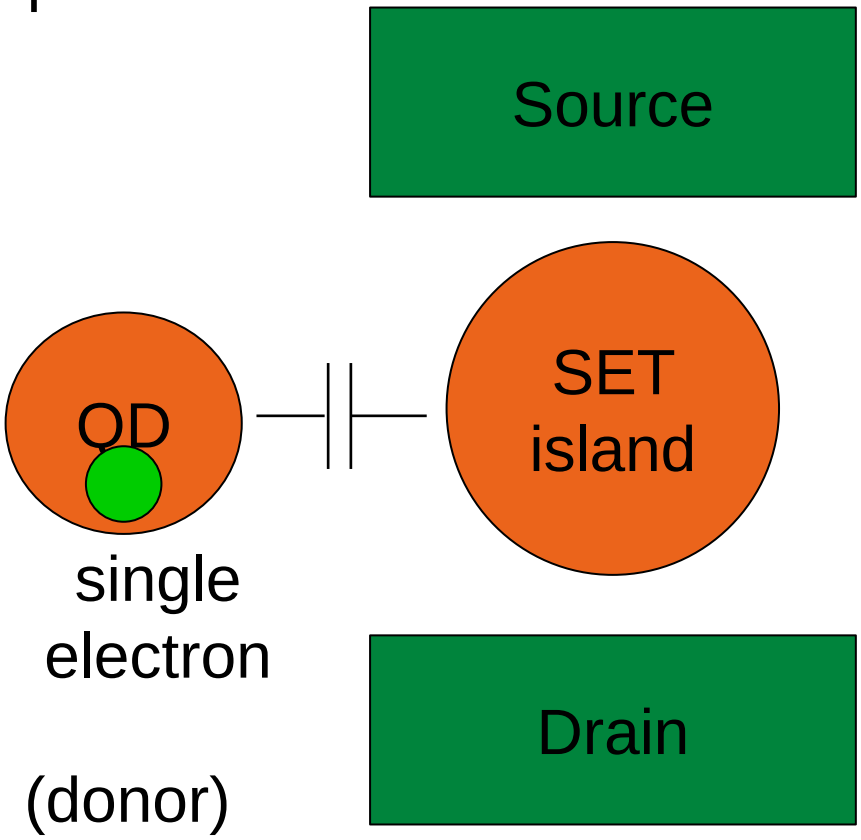


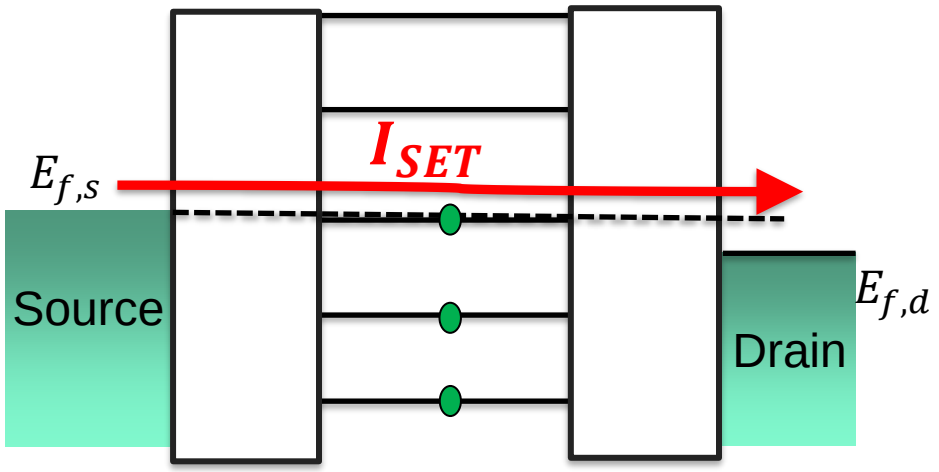


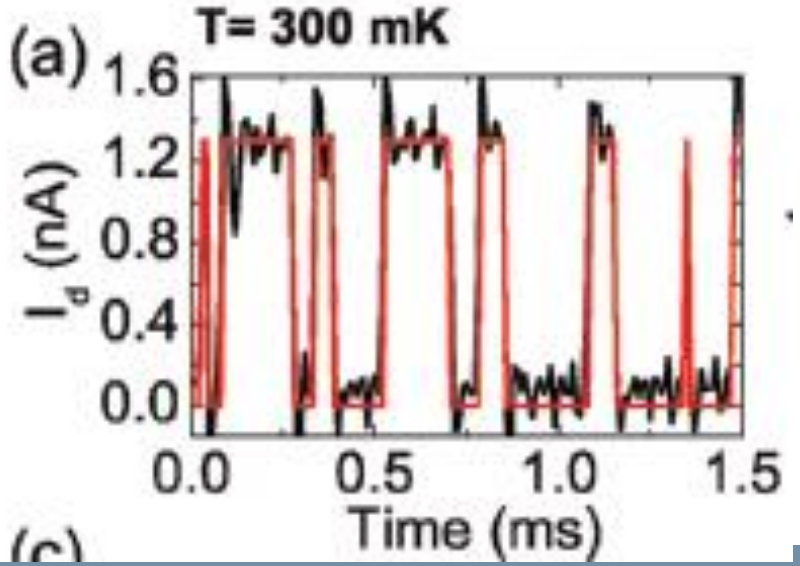
SET-based single-charge detector

Top view:



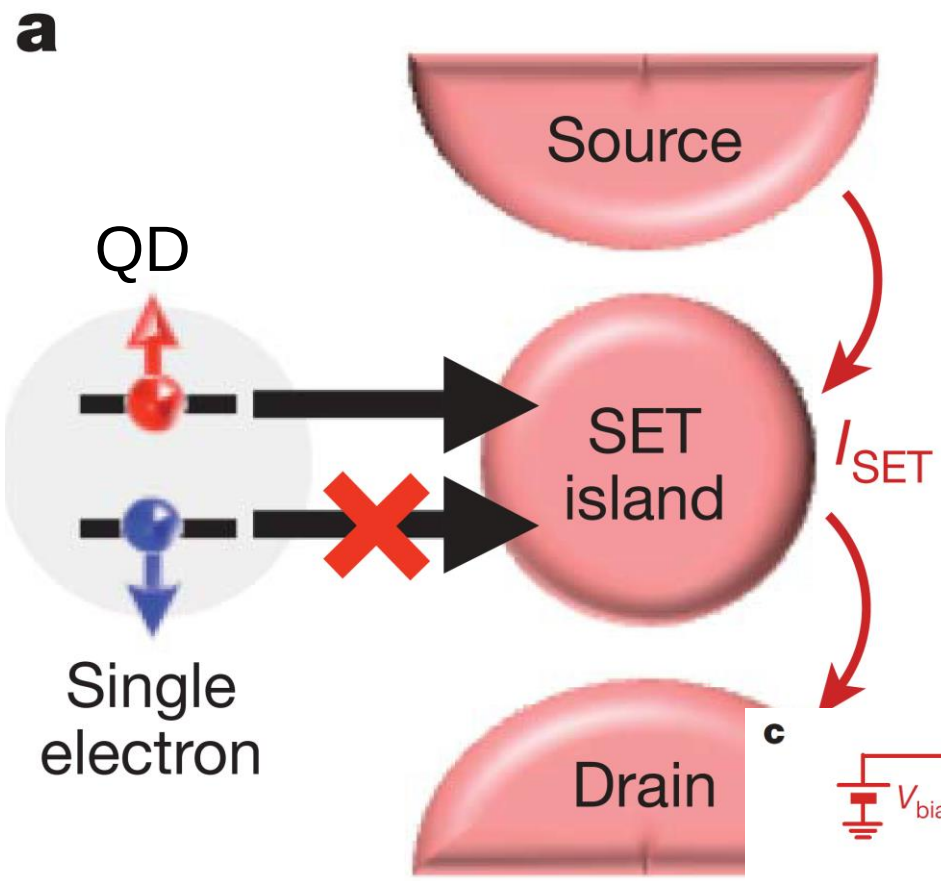
Energy levels:





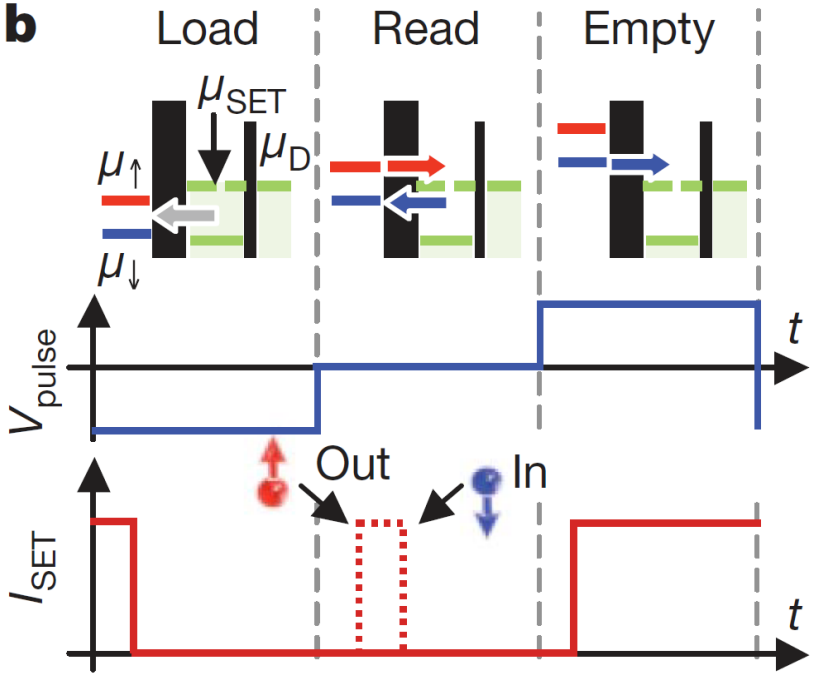
Mazzeo, Prati, Ferrari et al APL 2012

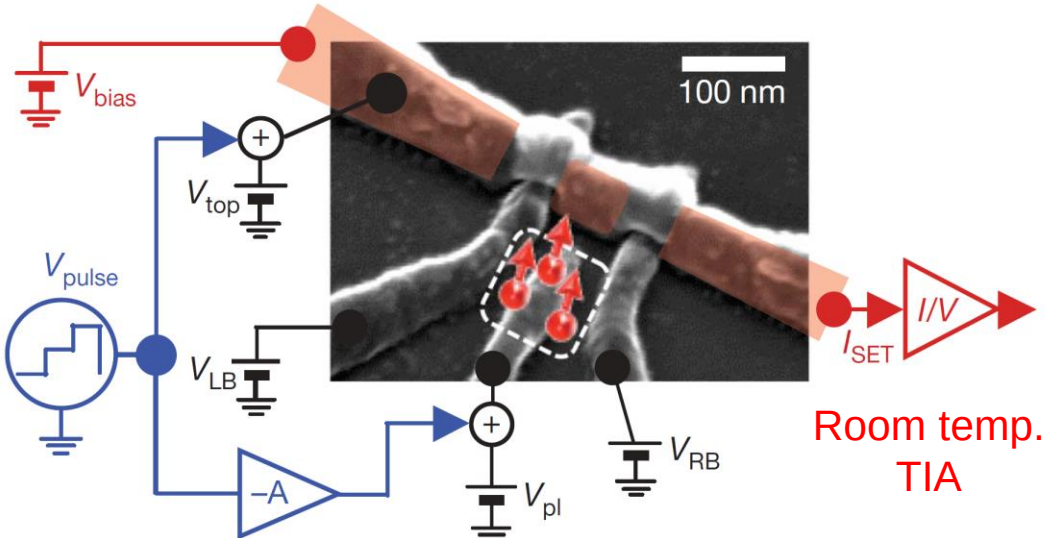
Spin state detection: spin-to-charge conversion



(alternative: a QPC)

electron → $I_{SET} \approx 0$
void → $I_{SET} > 0$

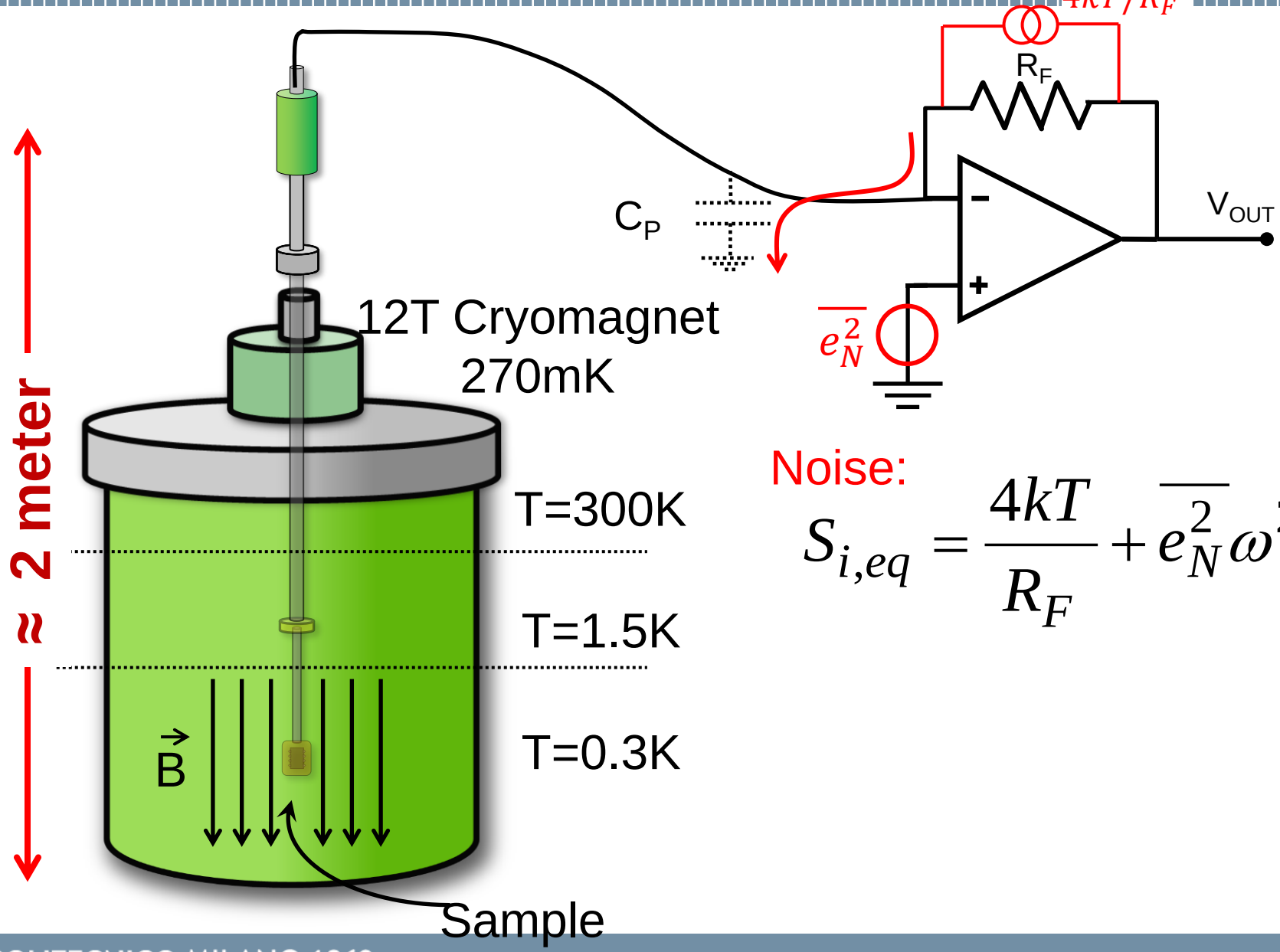




Room temp.
TIA

A. Morello,et al. *Nature*, no. 7316, pp. 687–91 2010, doi: 10.1038/nature09392.

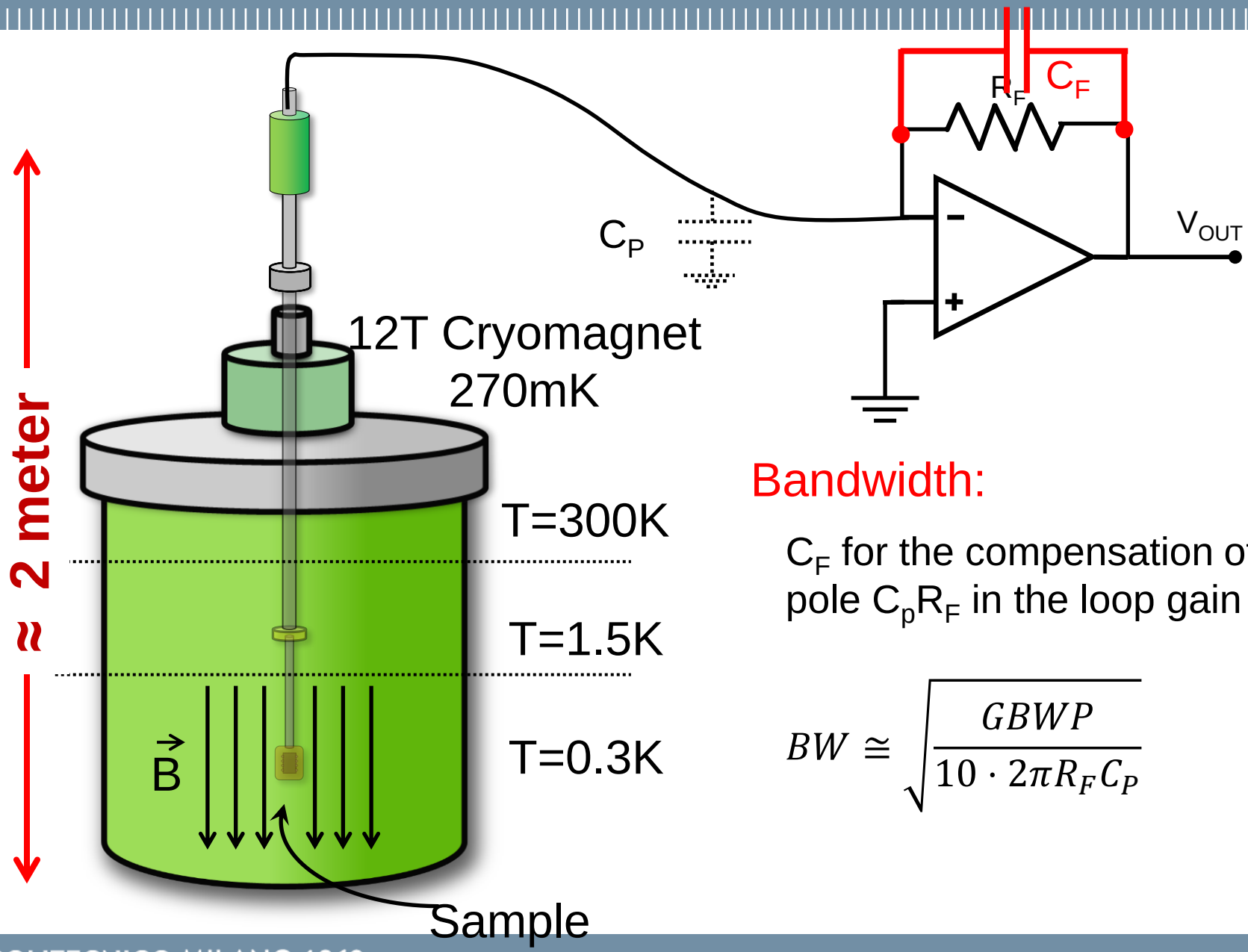
Experimental set-up to study quantum devices



Noise:

$$S_{i,eq} = \frac{4kT}{R_F} + \overline{e_N^2}\omega^2 C_P^2$$

Experimental set-up to study quantum devices

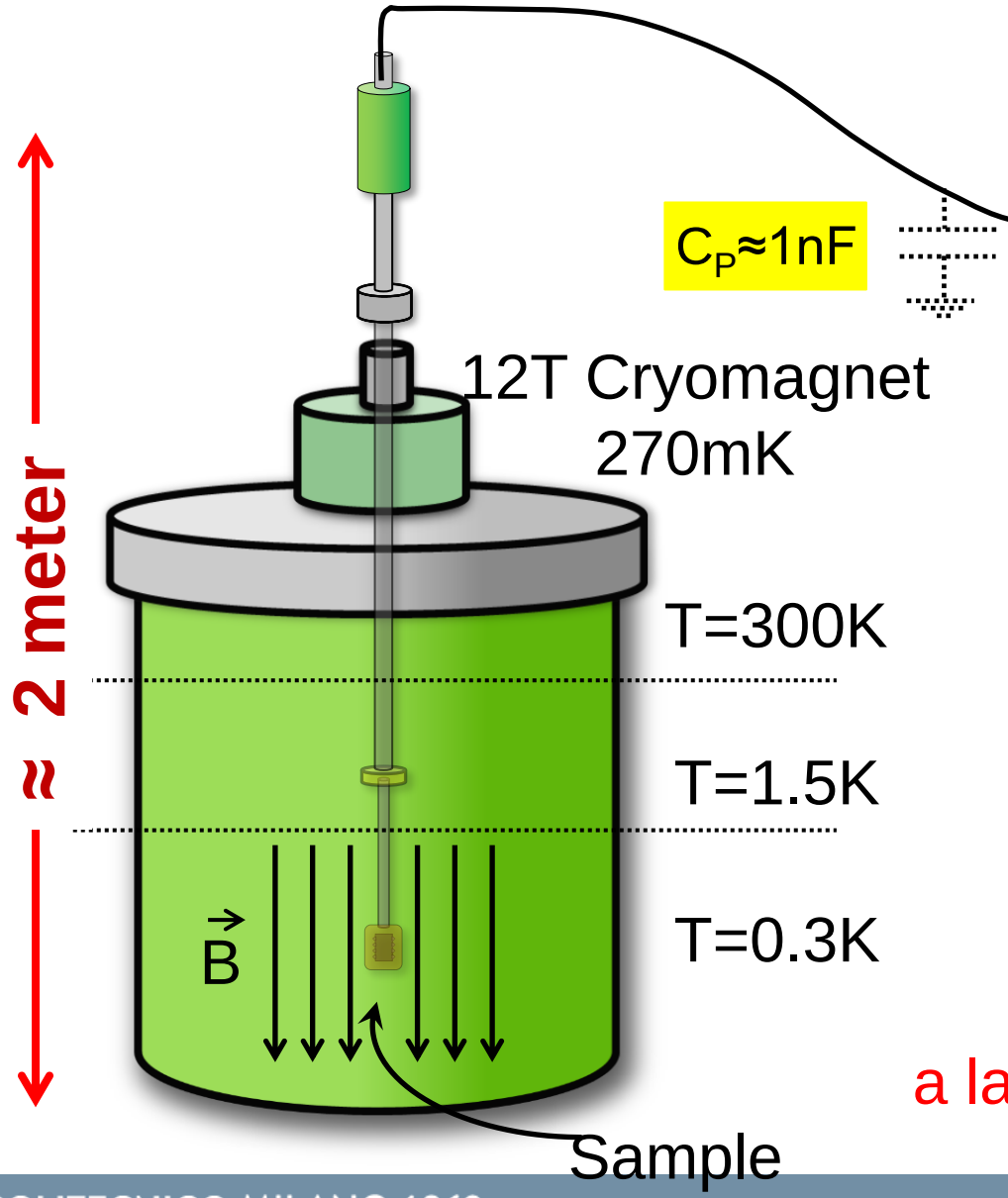


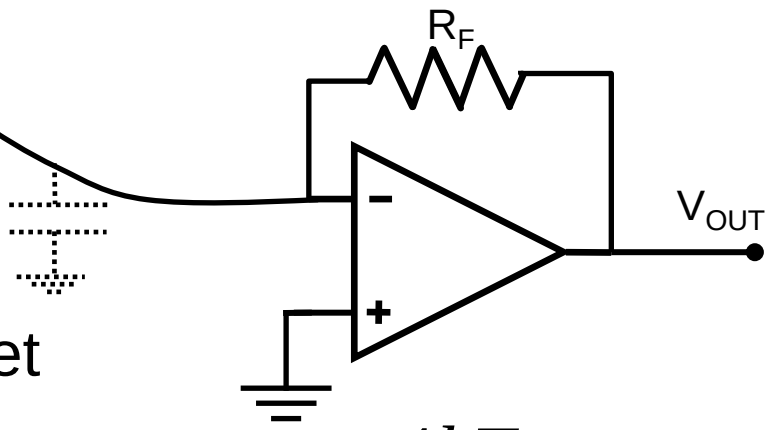
Bandwidth:

C_F for the compensation of the pole C_pR_F in the loop gain

$$BW \cong \sqrt{\frac{GBWP}{10 \cdot 2\pi R_F C_P}}$$

Experimental set-up to study quantum devices





$$S_{i,eq} = \frac{4kT}{R_F} + \overline{e_N^2}\omega^2 C_P^2$$

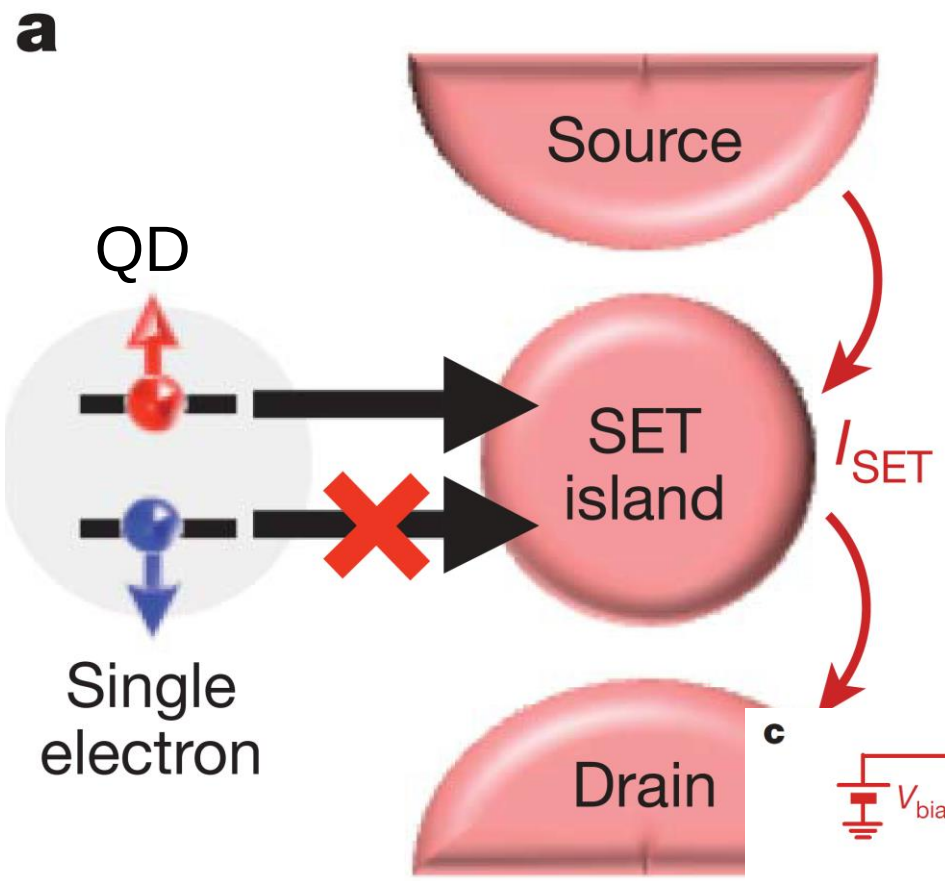
$$I_{RMS} = \frac{2\pi e_N C_P BW^{3/2}}{\sqrt{3}}$$

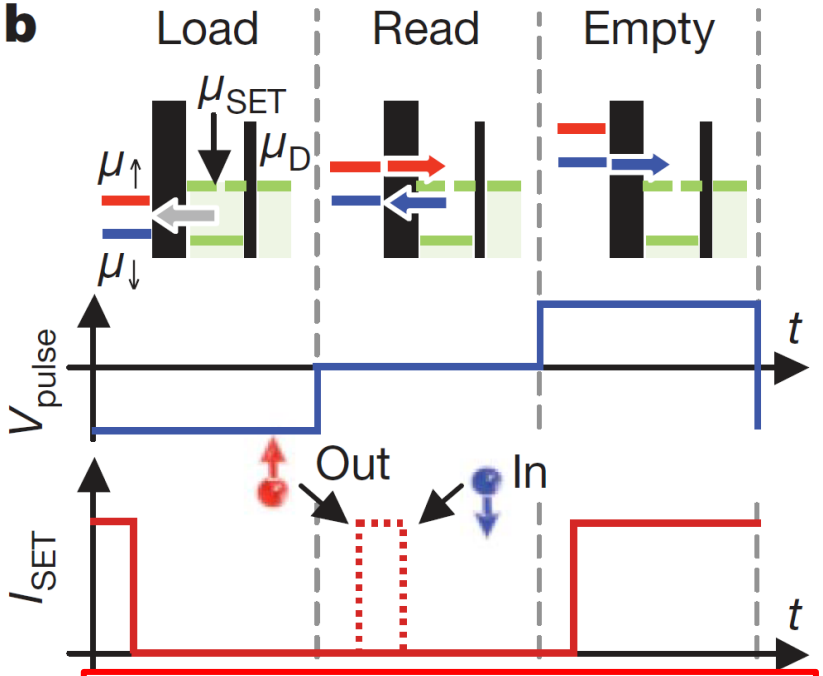
$$BW = \sqrt{\frac{GBWP}{10 \cdot 2\pi R_F C_P}}$$

a large C_P reduces performances

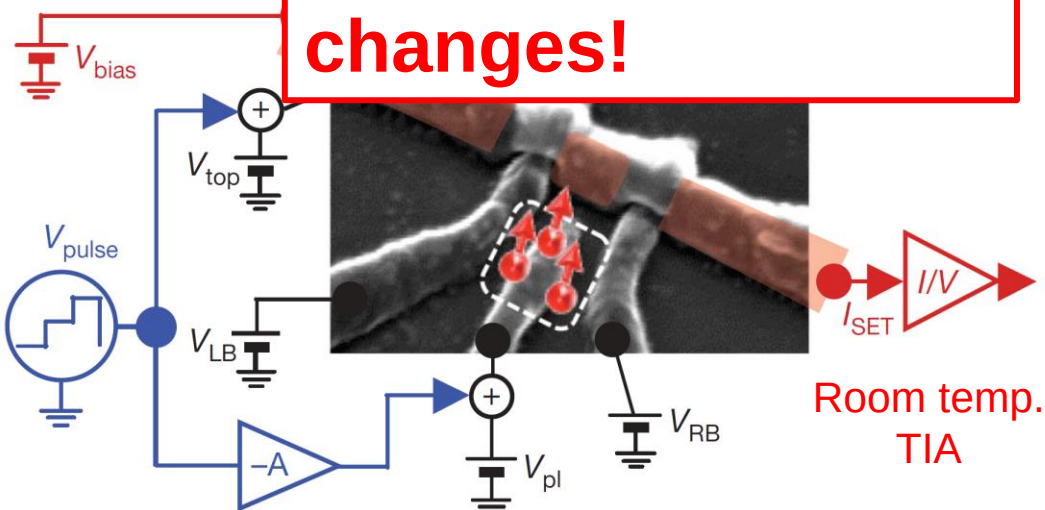
R_F=10MΩ: BW=40kHz, 150pArms

Spin state detection: spin-to-charge conversion





The SET resistance changes!



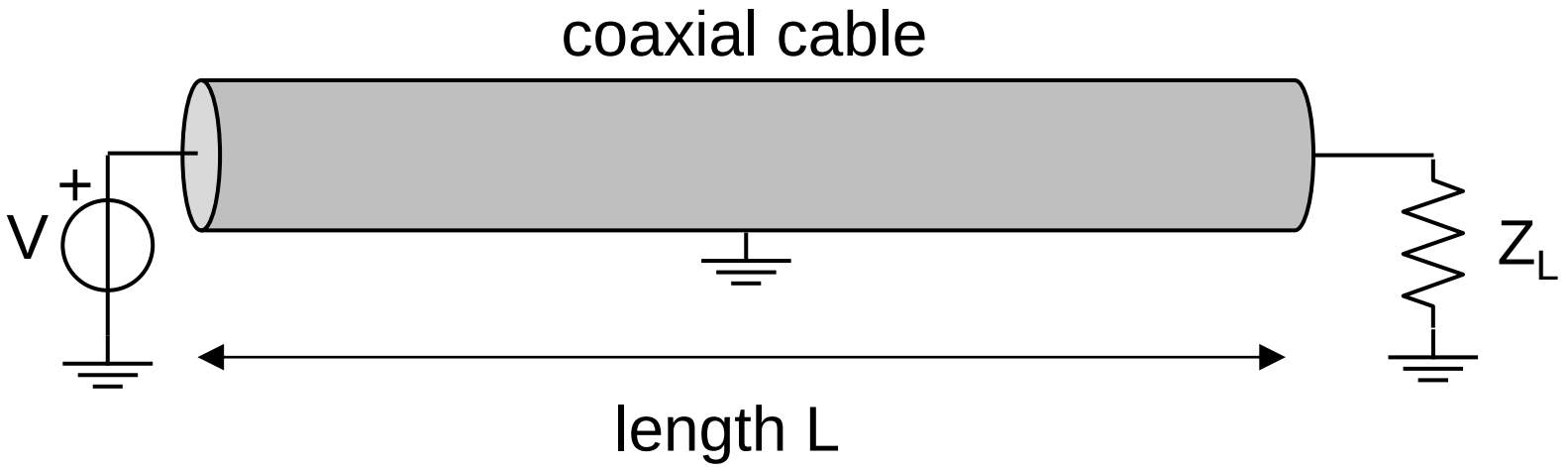
Room temp. TIA

electron → $I_{SET} \approx 0$
void → $I_{SET} > 0$

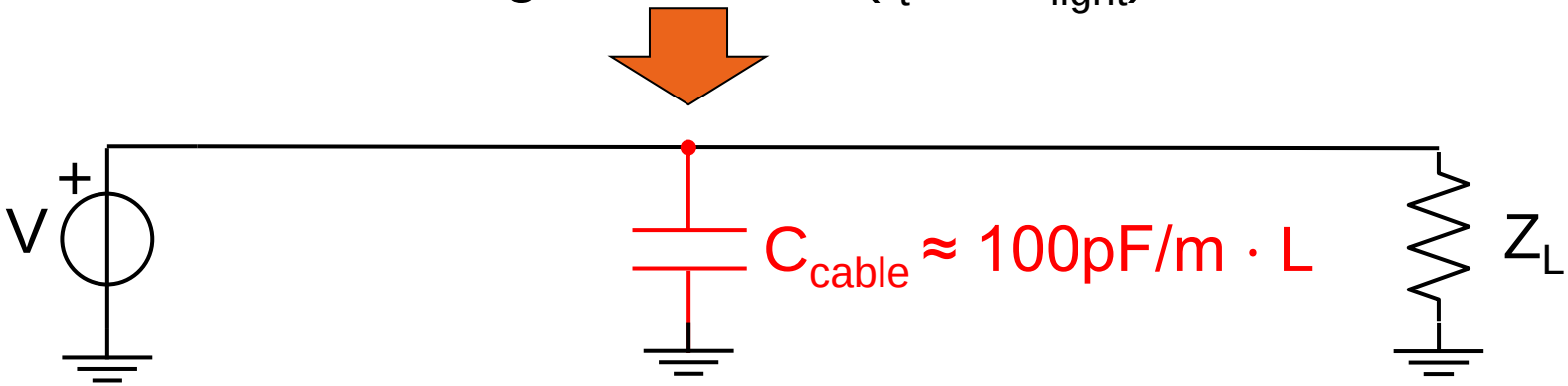
A. Morello,et al. *Nature*, no. 7316, pp. 687–91 2010, doi: 10.1038/nature09392.

How to avoid being penalized by a long cable?

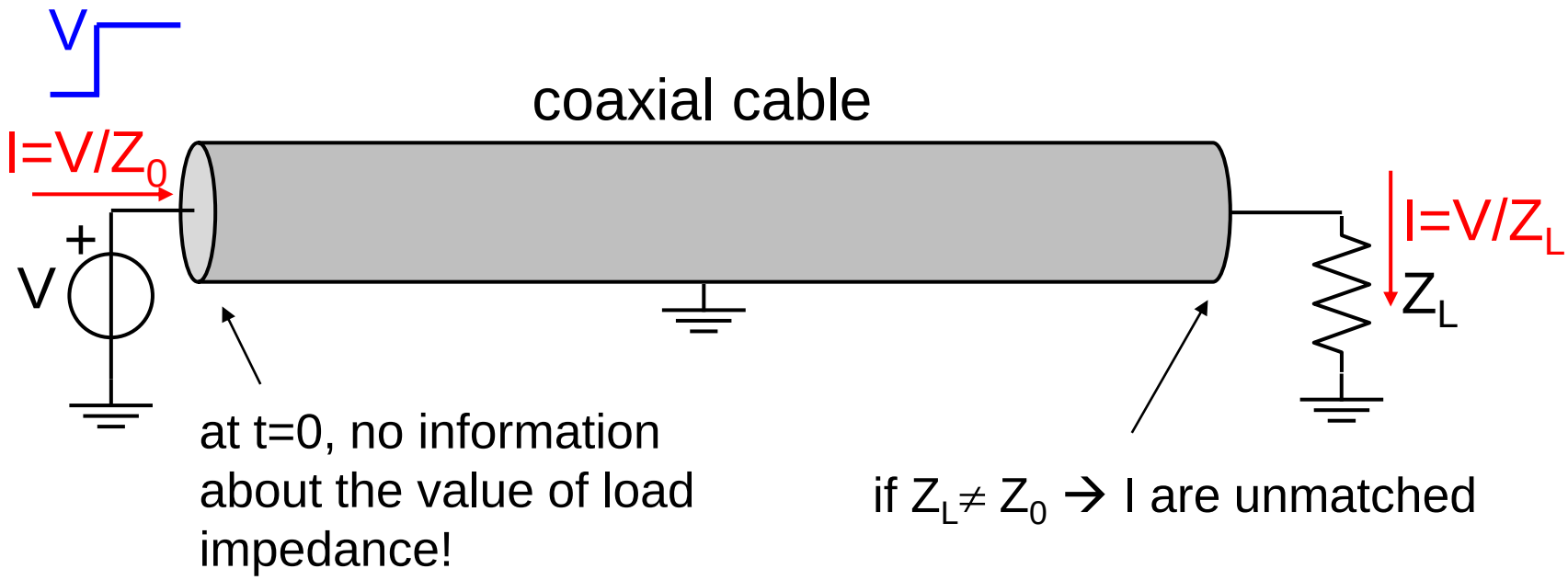
Measuring an impedance using the properties of the cable:



If V changes slowly compared to the transit time of the electromagnetic wave ($t_t = L/v_{light}$):

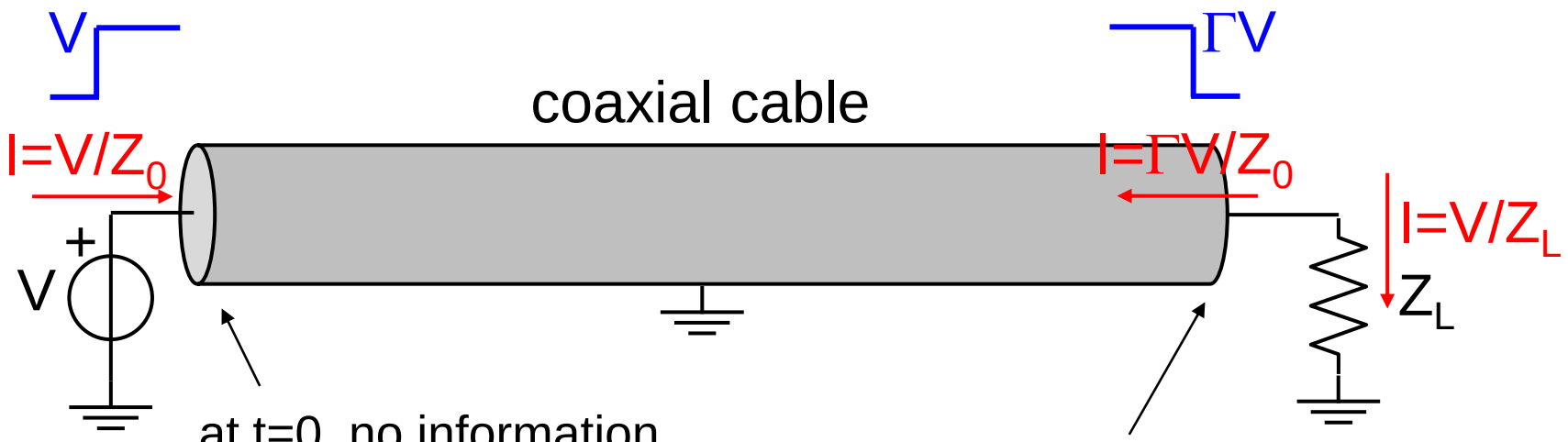


Transmission line



Z_0 = characteristic impedance of the cable, usually 50Ω

Transmission line



Z_0 = characteristic impedance of the cable, usually 50Ω

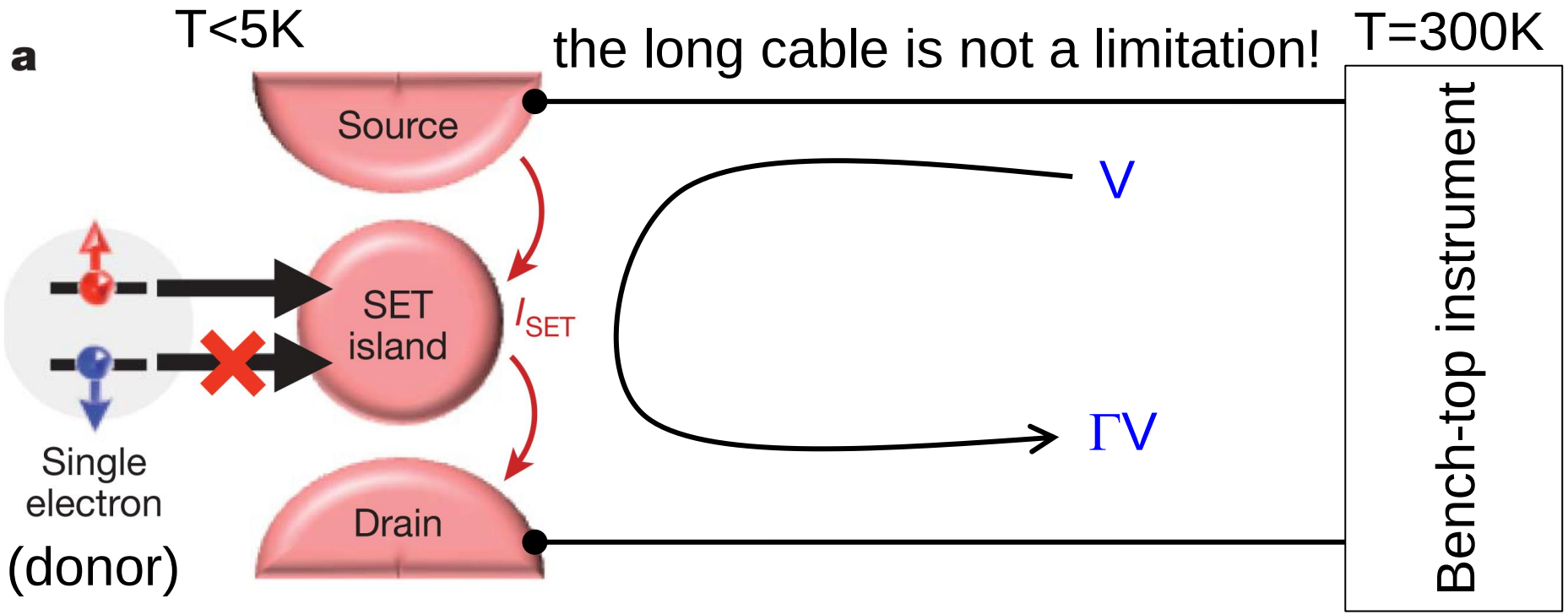
The reflected wave is related to the load impedance!

a reflected wave is created!

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

reflection coefficient

Radio-frequency spin readout

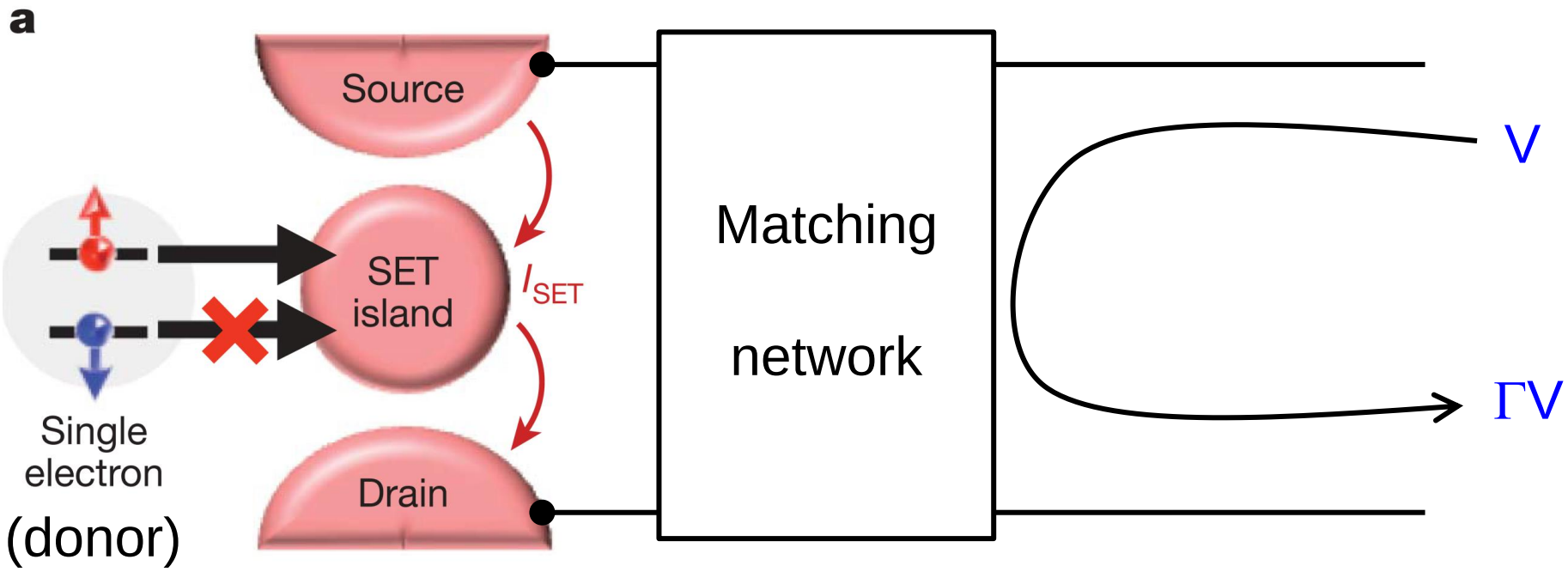


SET resistance depends on the donor charge that, in turn, depends on the spin

$$\Gamma = \frac{R_{SET} - Z_0}{R_{SET} + Z_0}$$

However, R_{SET}>25kΩ, Z_0≈ 50Ω ⇒ limited sensitivity

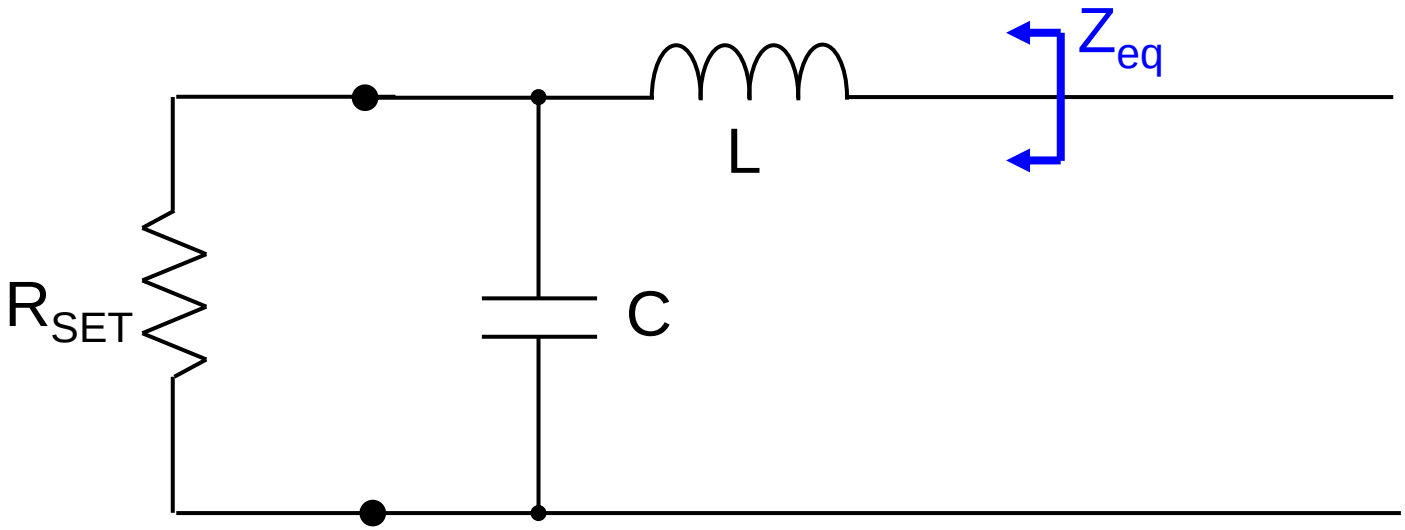
Matching network



SET resistance depends by the donor charge

Passive network to match the high resistance of the SET to the Z_0=50Ω of the line

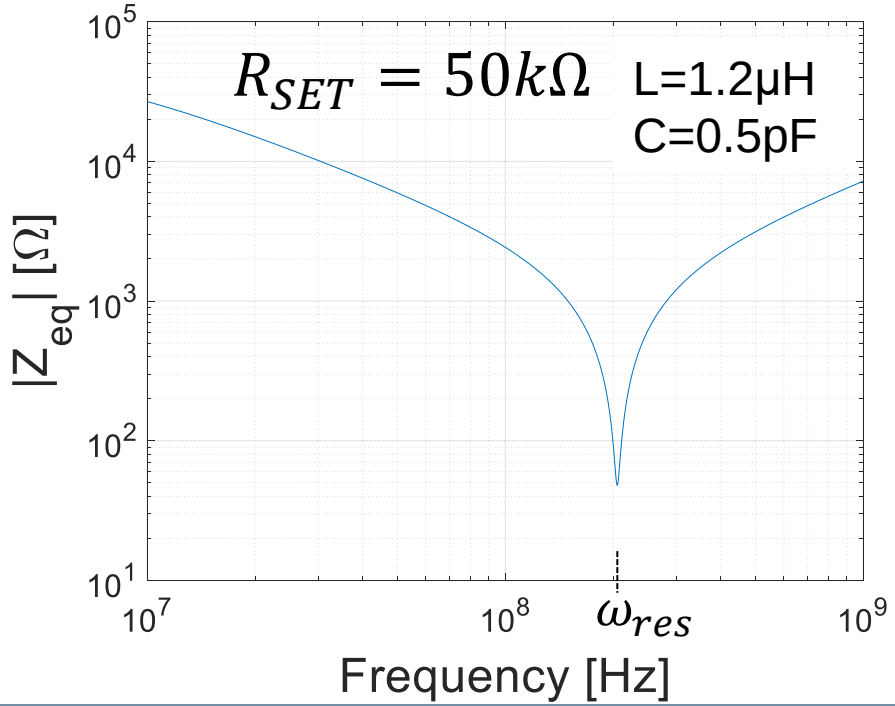
Matching network



$$Z_{eq} = R_{SET}\frac{1 + \frac{sL}{R_{SET}} + s^2LC}{1 + sCR_{SET}}$$

$$\omega_{res} = \frac{1}{\sqrt{LC}}$$

$$Z_{eq}(\omega_{res}) = \frac{L}{CR_{SET}}$$



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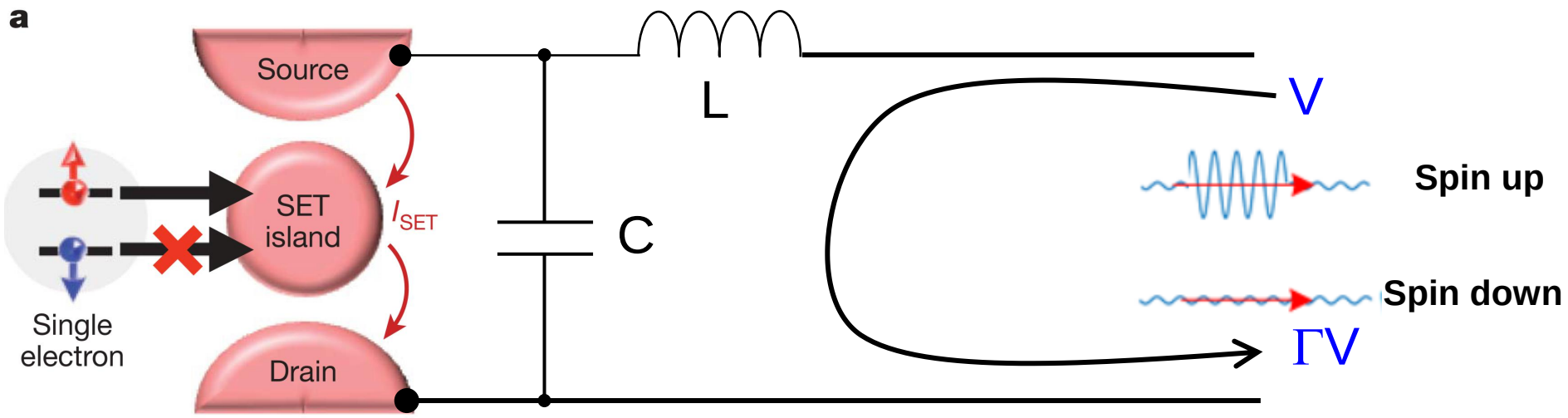
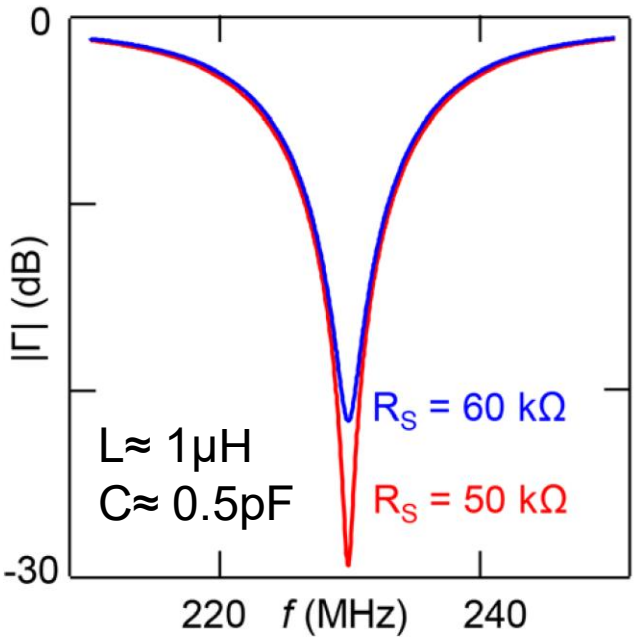


$$\Gamma(\omega_{res}) = \frac{Z_{eq}(\omega_{res}) - Z_0}{Z_{eq}(\omega_{res}) + Z_0}$$

L,C selected to have $Z_L(\omega_{res}) \approx Z_0$

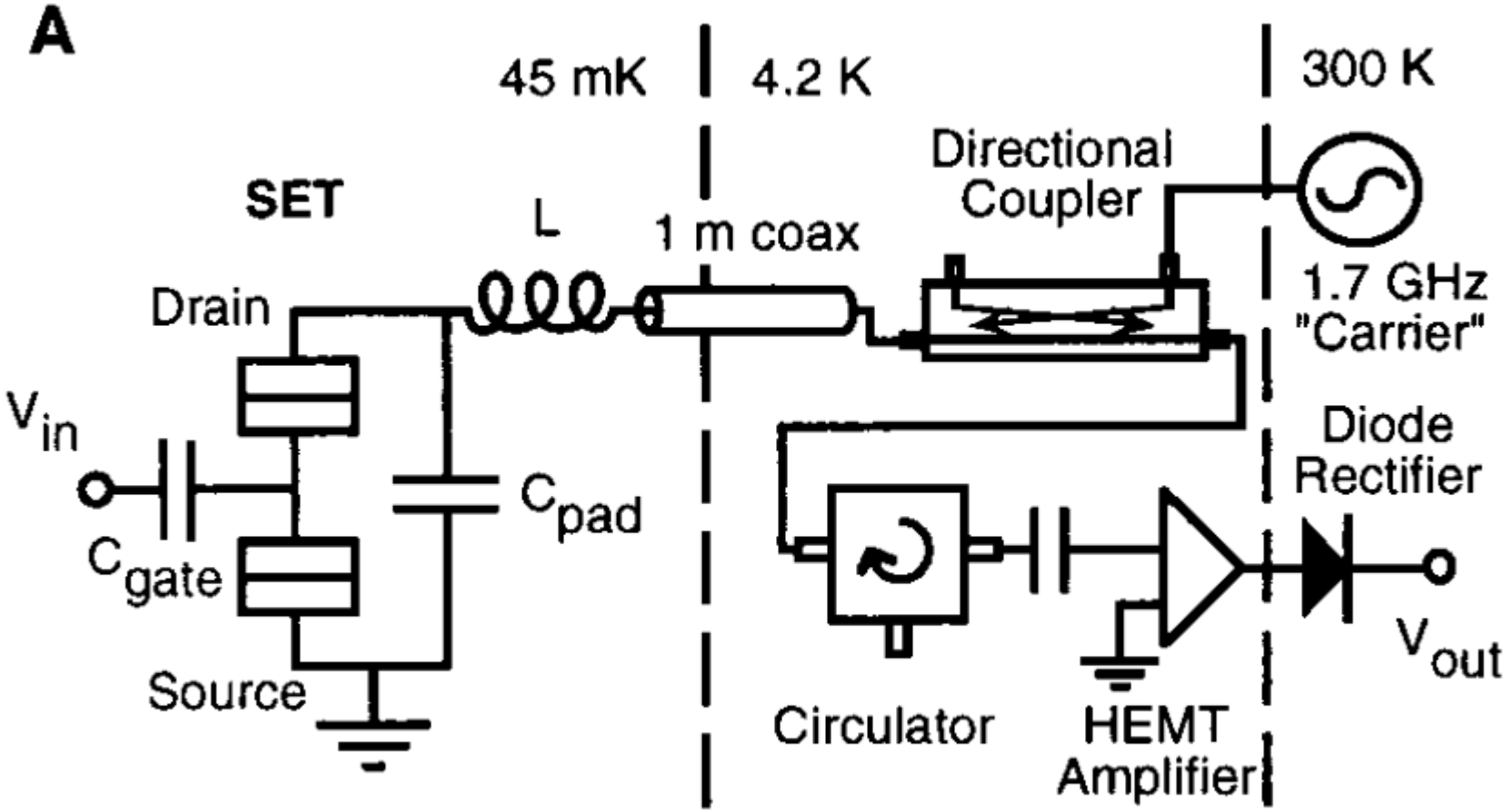
$$Z_{eq}(\omega_{res}) = \frac{L}{CR_{SET}}$$



F. Vigneau, et al. *Appl. Phys. Rev.* (2023), doi: 10.1063/5.0088229.

Readout based on RF reflectometry

R. Schoelkopf, et al. “The radio-frequency single-electron transistor (RF-SET): A fast and ultrasensitive electrometer,” *Science*, vol. 280, no. 5367, pp. 1238–42, May 1998



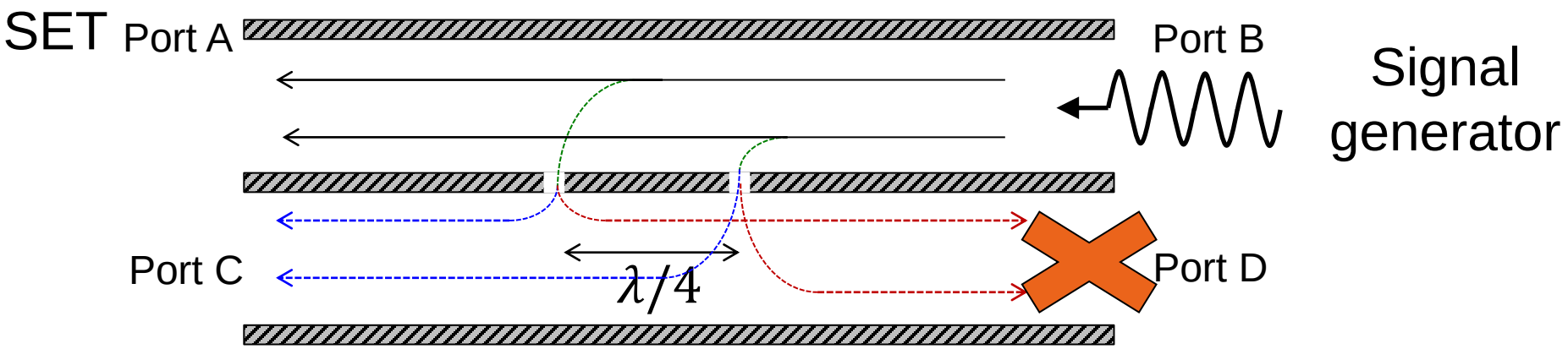
Reflectometry allows high-sensitivity impedance meas. despite long cables

(similar technique could be applied to the gate of the SET)

Recent review paper: F. Vigneau, et al. *Appl. Phys. Rev. (*2023), doi: 10.1063/5.0088229.

Directional coupler

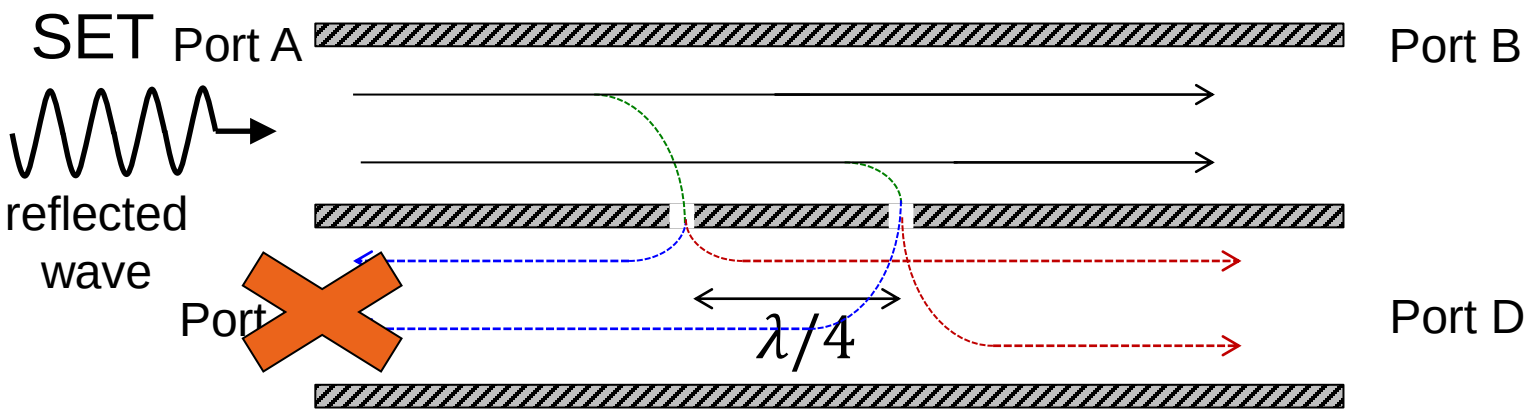
Basic idea using waveguides:



The contributions are added at port C.
However, since the paths differ in length by λ/2, they cancel at port D.

Directional coupler

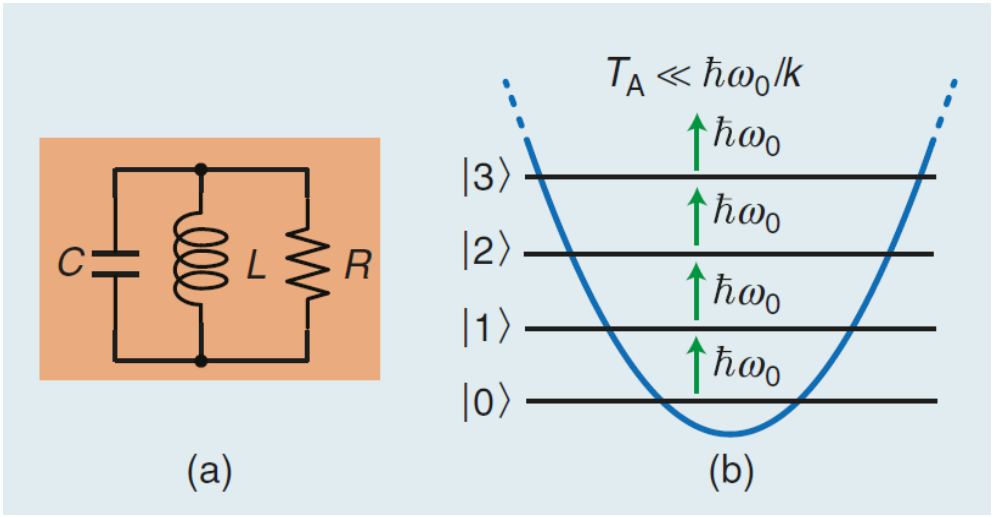
Basic idea using waveguides:



The only signal at port D is the reflected wave! (≪ voltage of the signal generator)

f=1GHz → λ ≈ 25cm

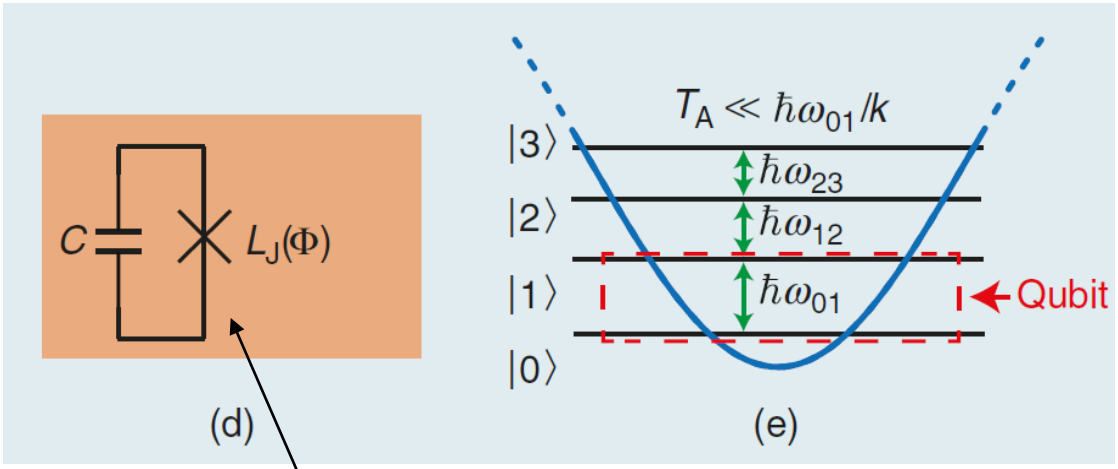
RF reflectometry for superconducting qubits



Standard linear resonator:

$$\hbar\omega_0 = 4\mu eV \ @1GHz$$
$$\rightarrow \ T < 50mK$$

ω_0 excites all the transitions



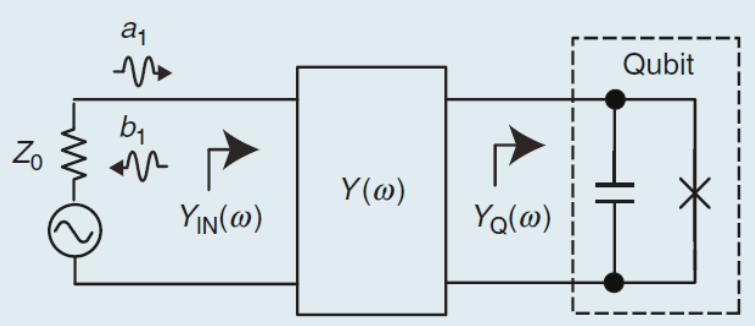
non-linear inductor
(Josephson junction)

non-linear resonator
→ nonuniform energy level spacing

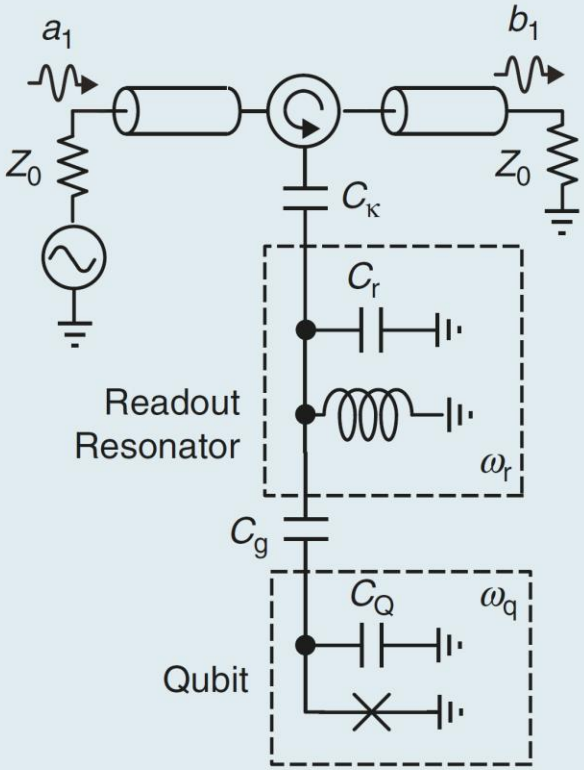
→ impedance depends on the oscillation amplitude, i.e. the qubit state!

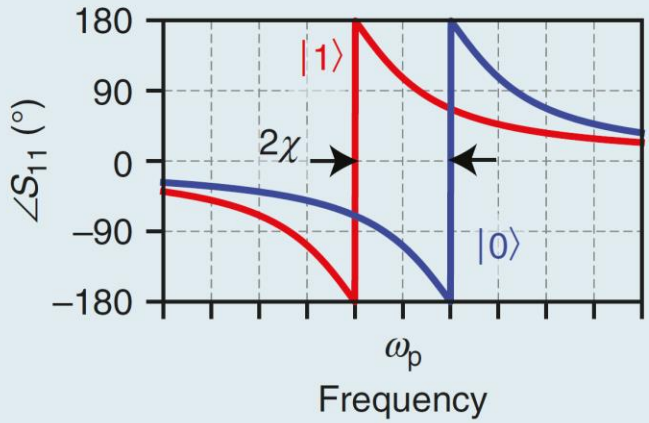
[J. Bardin et al, IEEE Microwave Magazine, 2020]

Readout of superconducting qubits

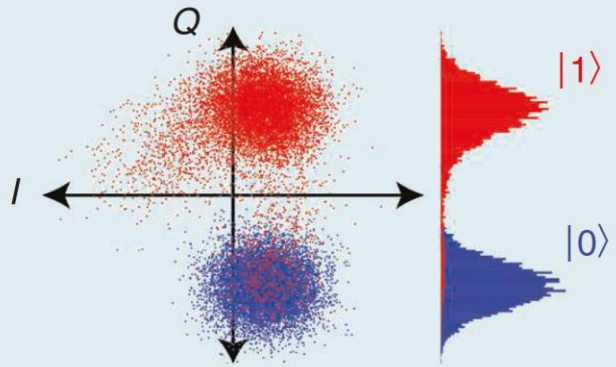


network Y(ω) for maximizing the signal and minimizing the perturbation on the qubit





(d)

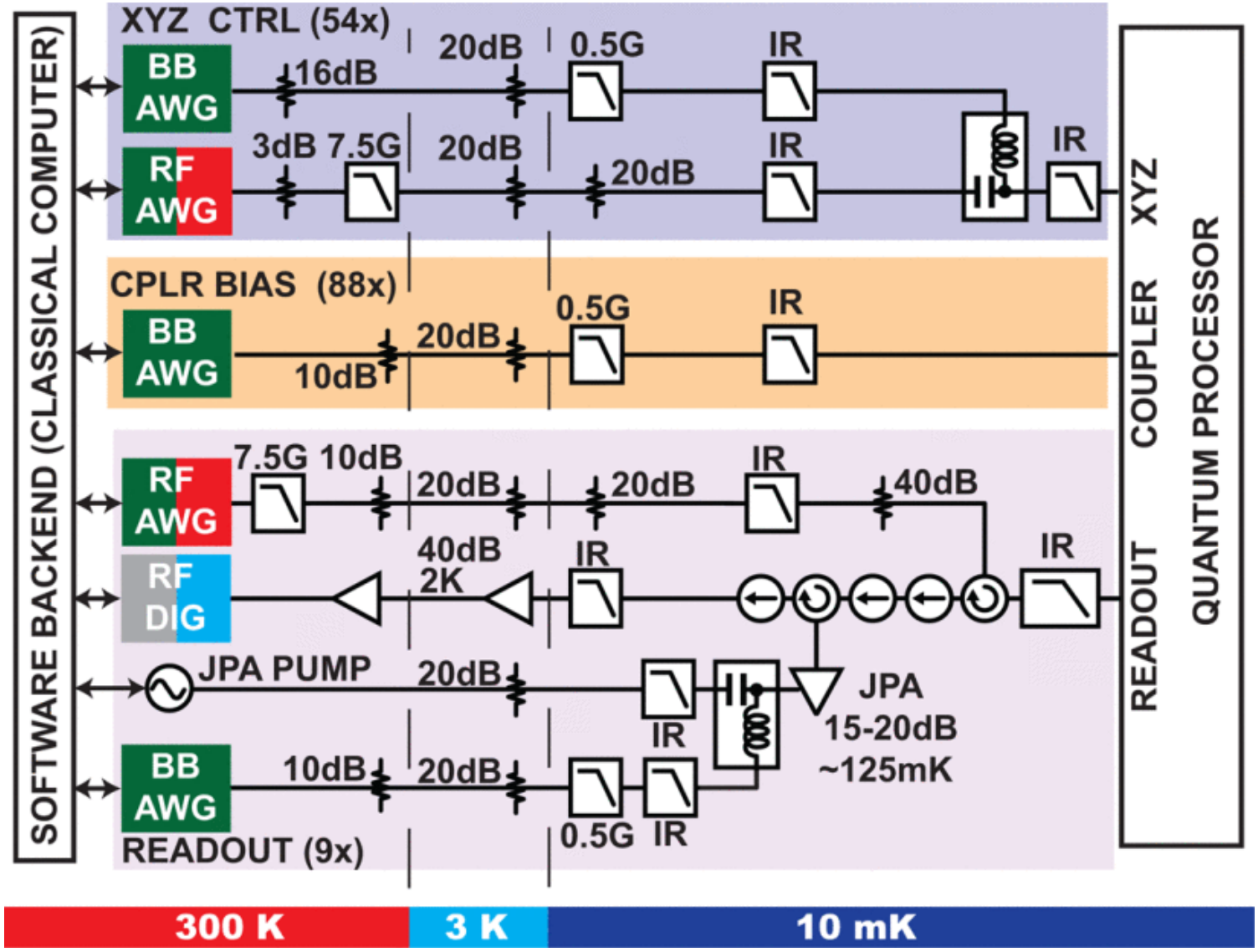


transmission line is not directly connected to the qubit

readout resonator freq. ≠ qubit resonator freq.

[J. Bardin et al, IEEE Microwave Magazine, 2020]

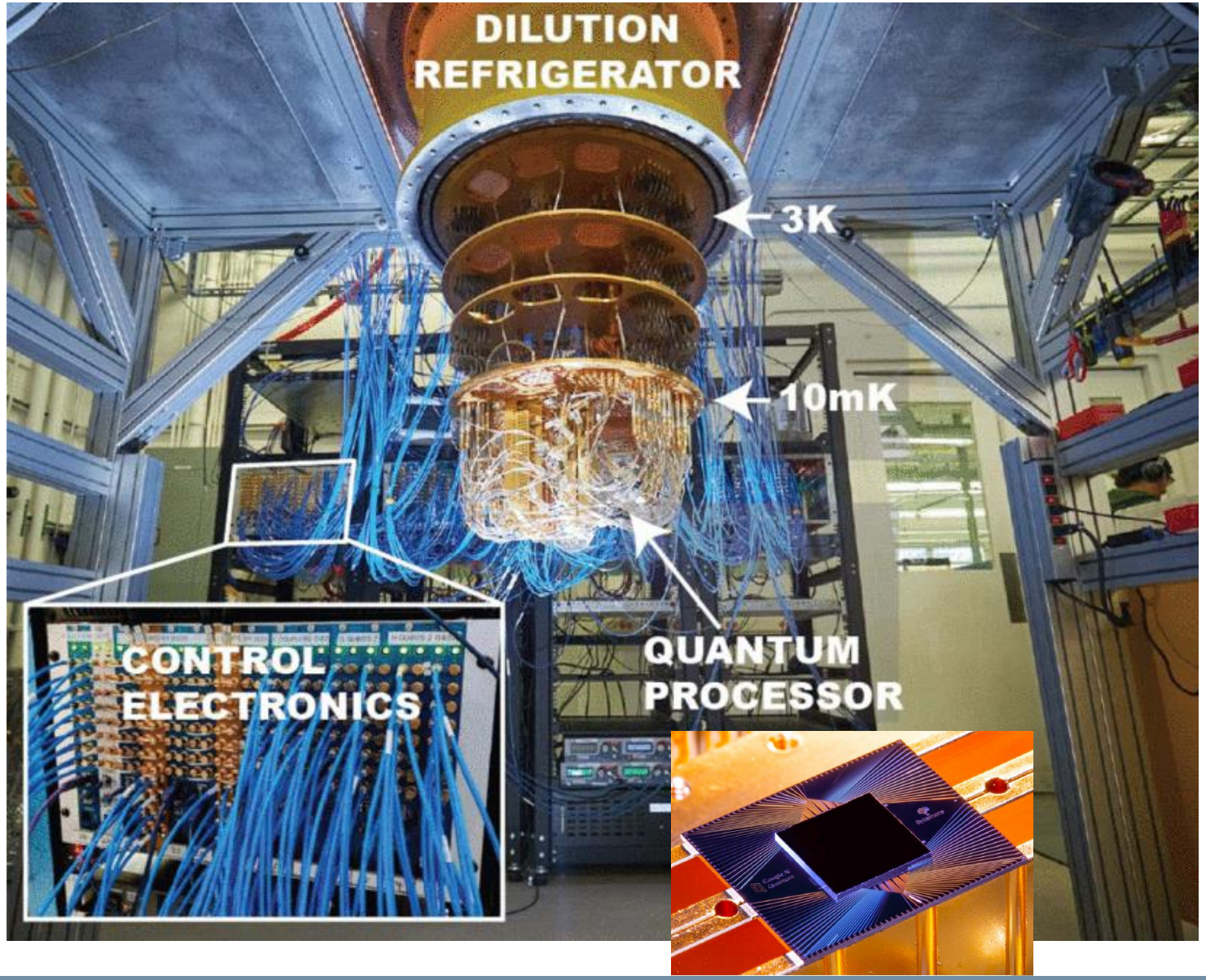
Google quantum computer (sycamore)



54 qubits (transmons)

[J. Bardin, ISSSCC 2022]

Google quantum computer (sycamore)



[J. Bardin, ISSSCC 2022]

Quantum computer: wiring!

MIT Technology Review

Intelligent Machines

We'd have more quantum computers if it weren't so hard to find the damn cables

by Martin Giles, January 17, 2019

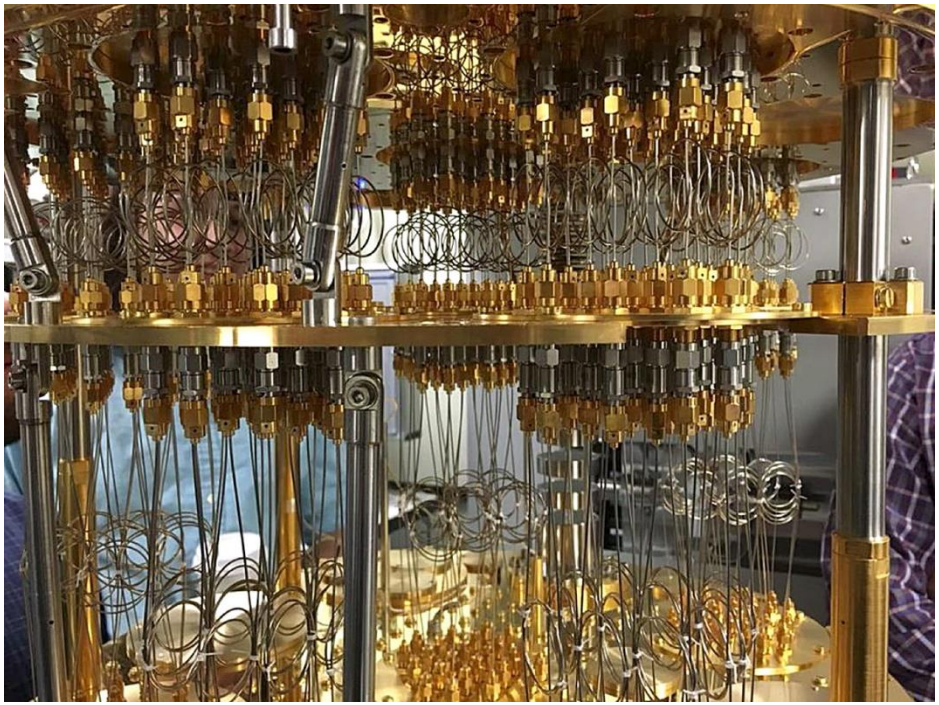
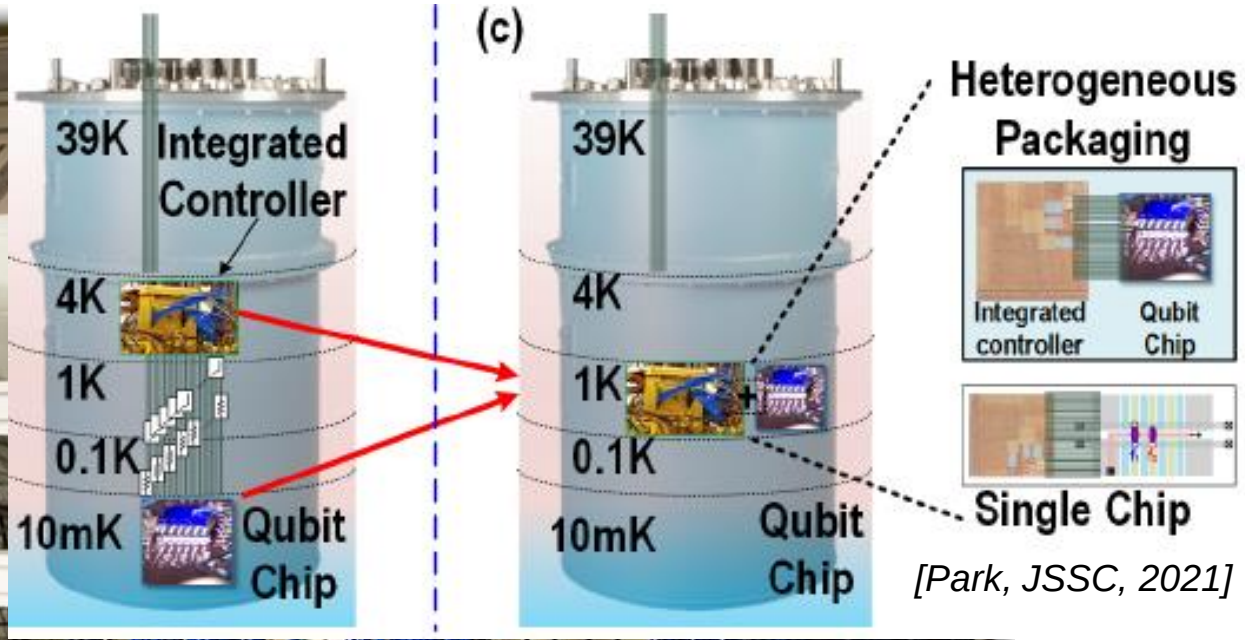


Image: IBM Research

Cables connecting qubits (<4K) to room temperature electronics are a limiting factor! (at least 2 coaxial cables / qubit)

- No space!
- No thermal budget! (≈1W at 4K, <1mW at 10mK)

Quantum computer: cryogenic electronics!



[Park, JSSC, 2021]

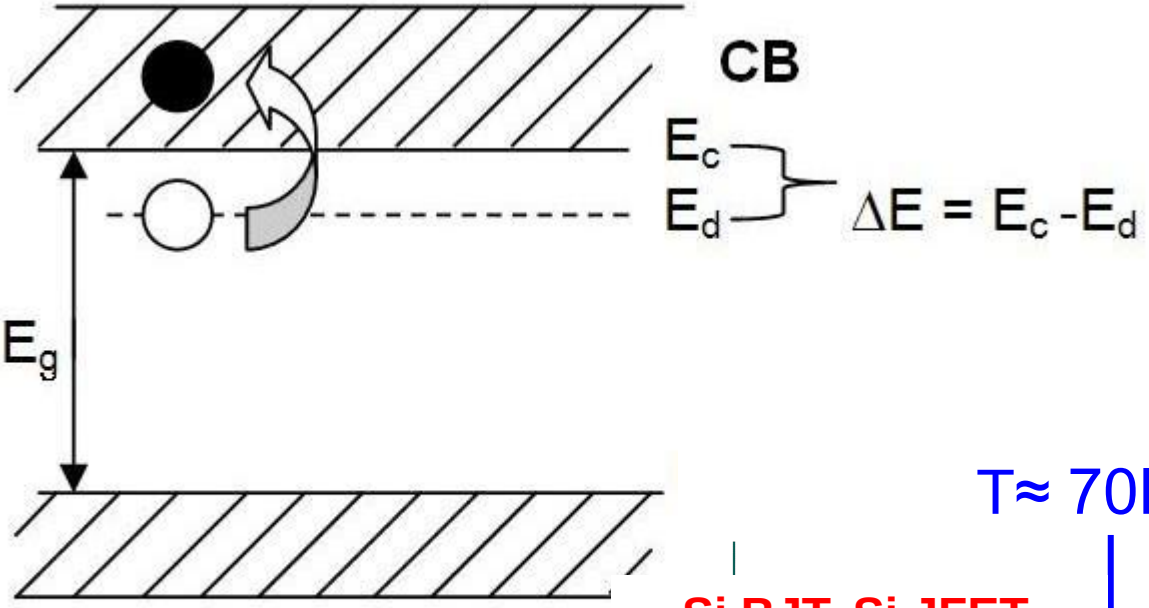
Readout and control electronics should be operated at cryogenic temperature, ideally on the same chip of the qubits, to minimize the number of cables!

[Bardin, ISSCC 2019]

Outline

- Spin detection using room temperature instrumentation
- Cryogenic electronics
  - Challenges
  - Design rules
- Examples

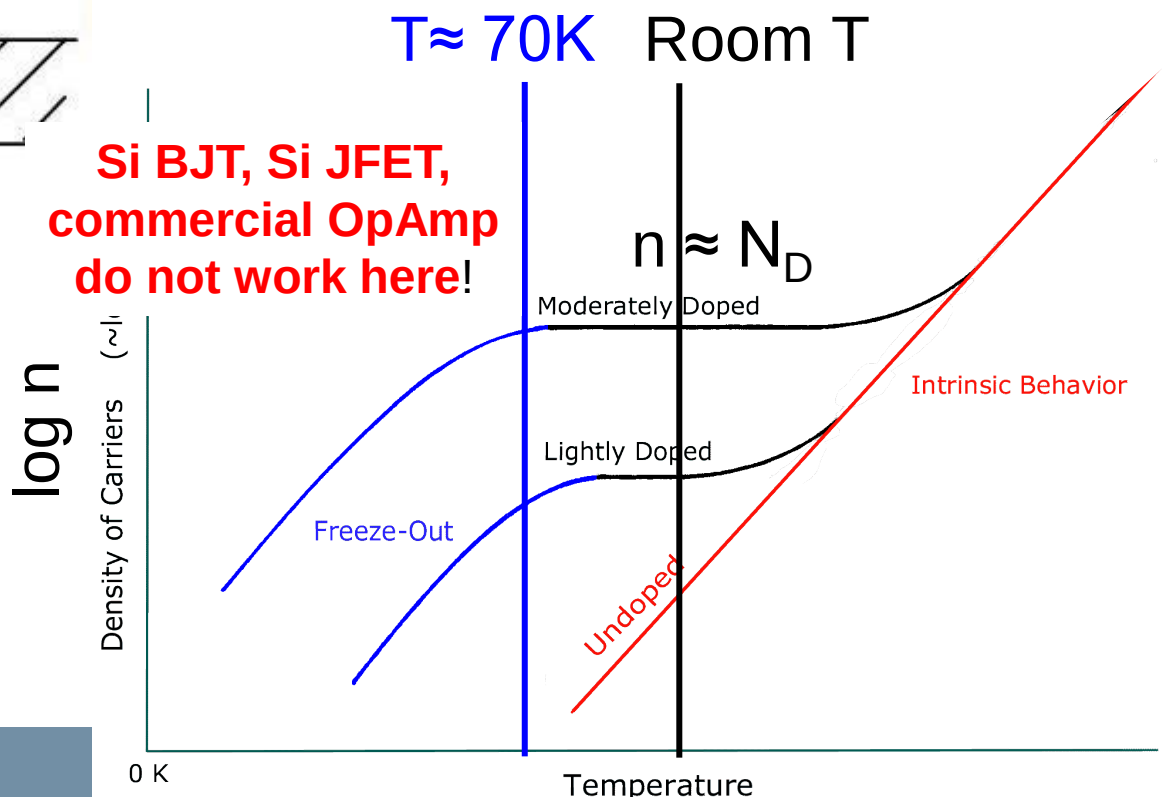
Semiconductor freeze-out



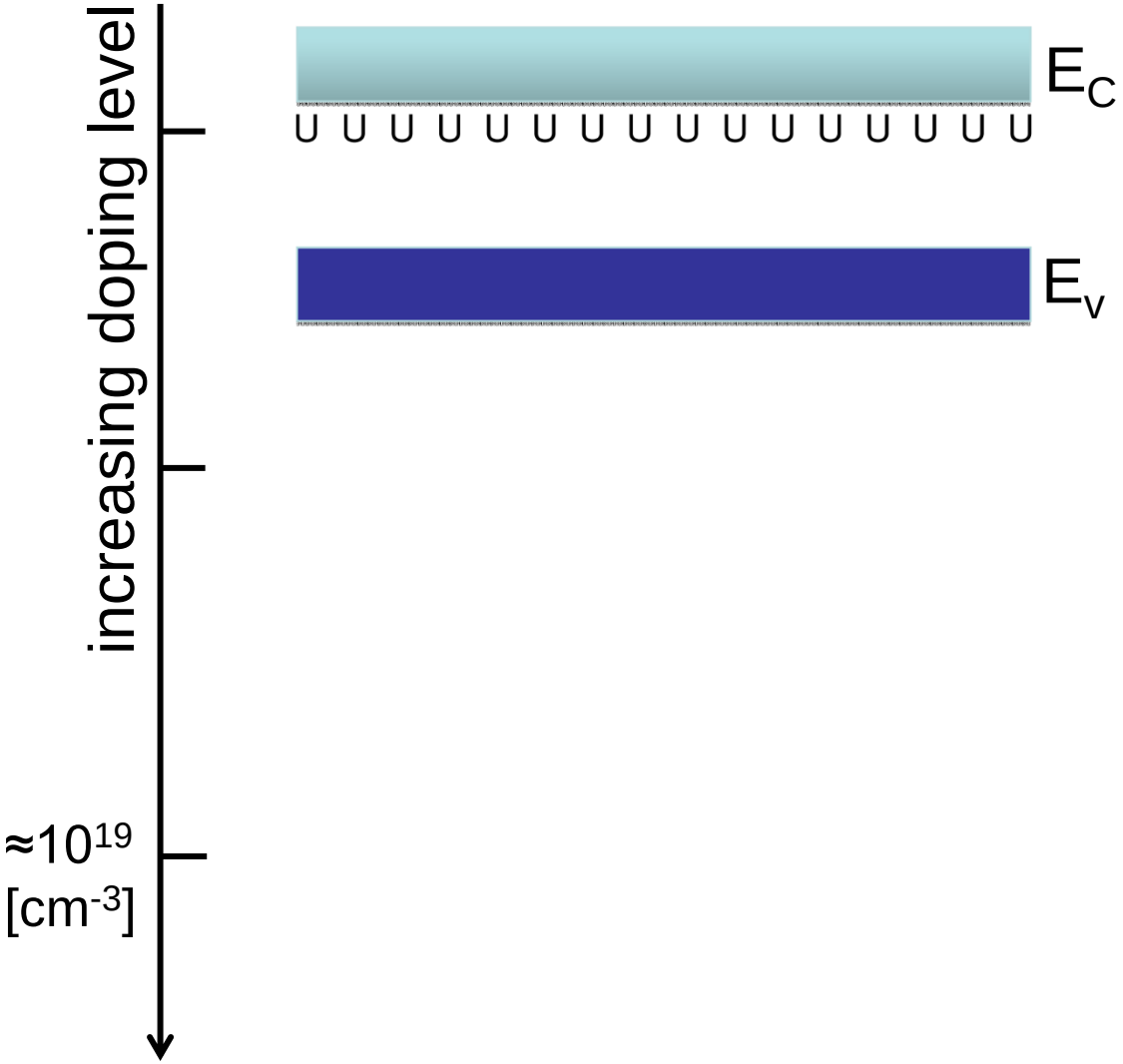
ionization energy for phosphorus: 45meV

$kT|_{70K}$= 6meV

http://fog.ccsf.cc.ca.us/~wkaufmyn/



The impurity band model



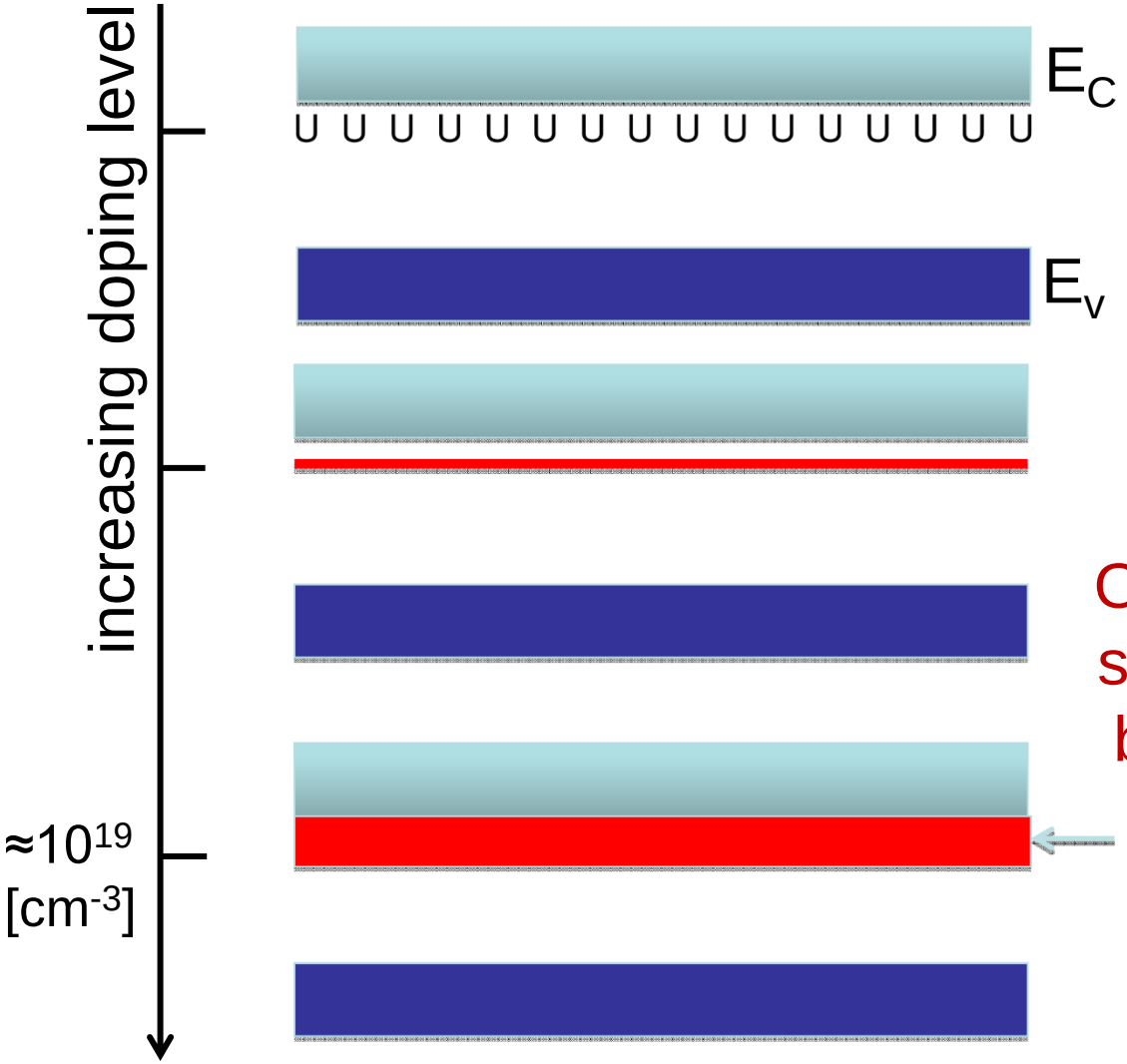
Akturk et al., Silicon qubit workshop, 2009

A. Discrete States

*Esther Conwell, "Impurity Band Formation In Germanium and Silicon," Phys. Rev. **103(1)**,51(1956)

E. Prati, G. Ferrari et al., Nature Nanotechnology 7, 443–447 (2012)

The impurity band model



Akturk et al., Silicon qubit workshop, 2009

A. Discrete States

B. On-set of impurity band formation

Overlapping in degenerate semiconductor will make it behave more like a metal than a semiconductor

C. Broadening of the impurity band and overlap with the main band

*Esther Conwell, "Impurity Band Formation In Germanium and Silicon," Phys. Rev. **103(1)**,51(1956)

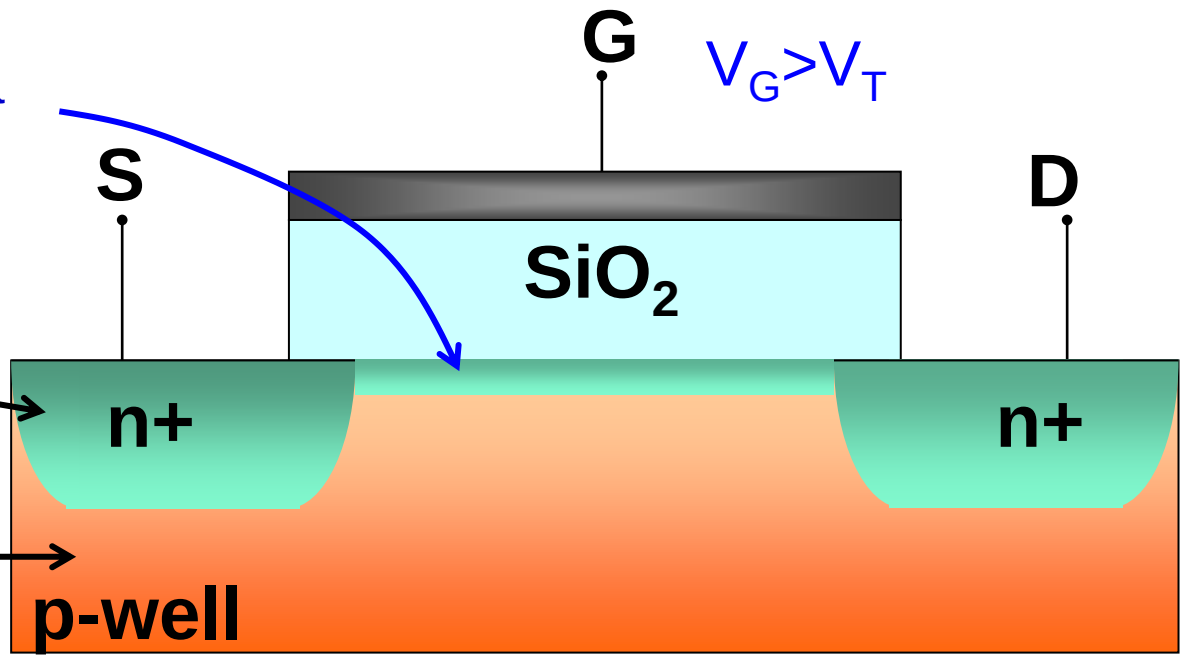
E. Prati, G. Ferrari et al., Nature Nanotechnology 7, 443–447 (2012)

Electronics below the freeze-out temp.

electric field creates a conductive channel!

no freeze-out: conductive

freeze-out: insulator

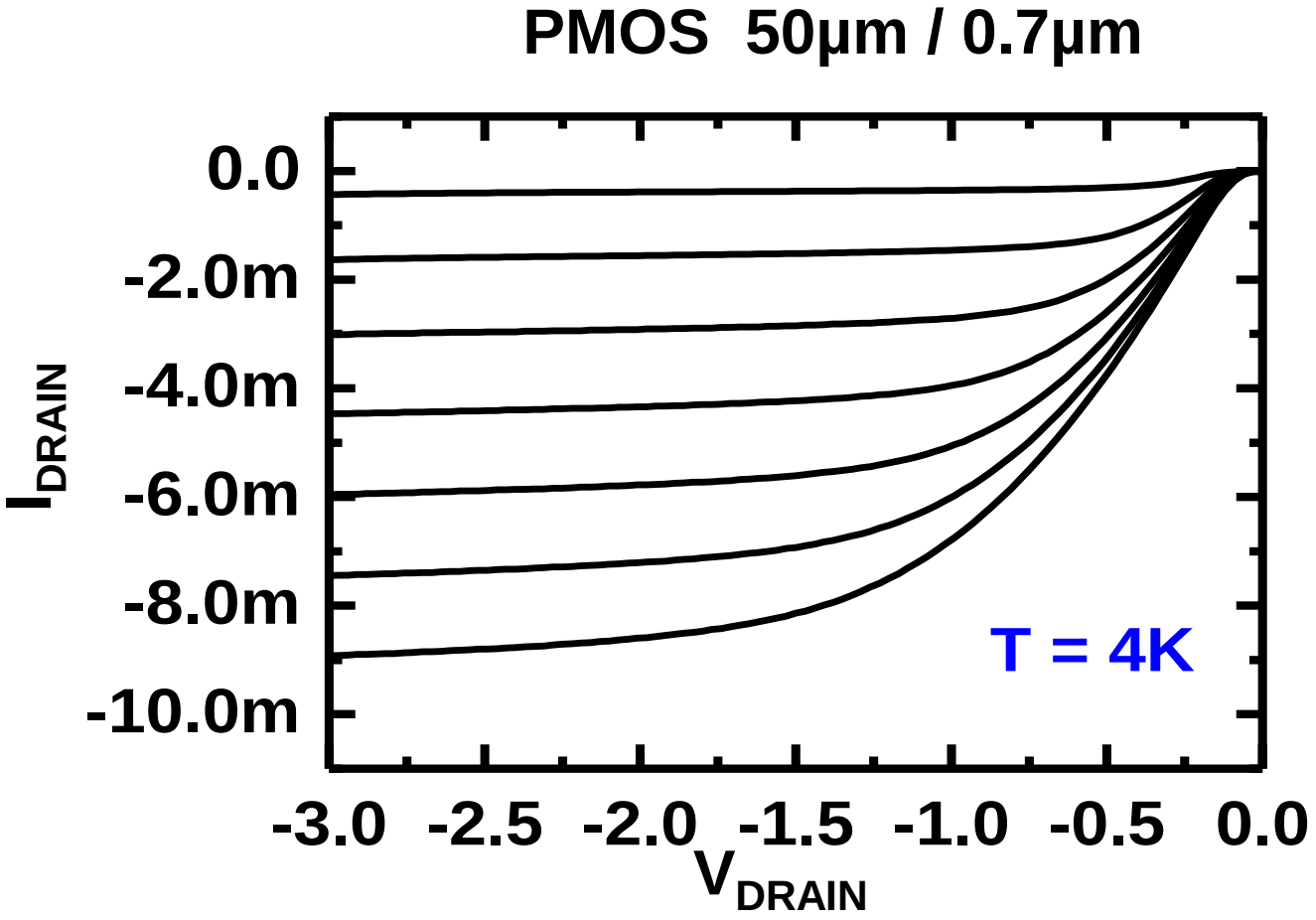


Silicon (standard) MOSFET operates below 40K!

Many GaAs devices operate at cryogenic temperature:
degenerate at 10^{16} cm^{-3}
Limitation: small (and expensive) scale integration

MOSFET operating at 4K

Standard analog CMOS Technology 3.3V, 0.35µm

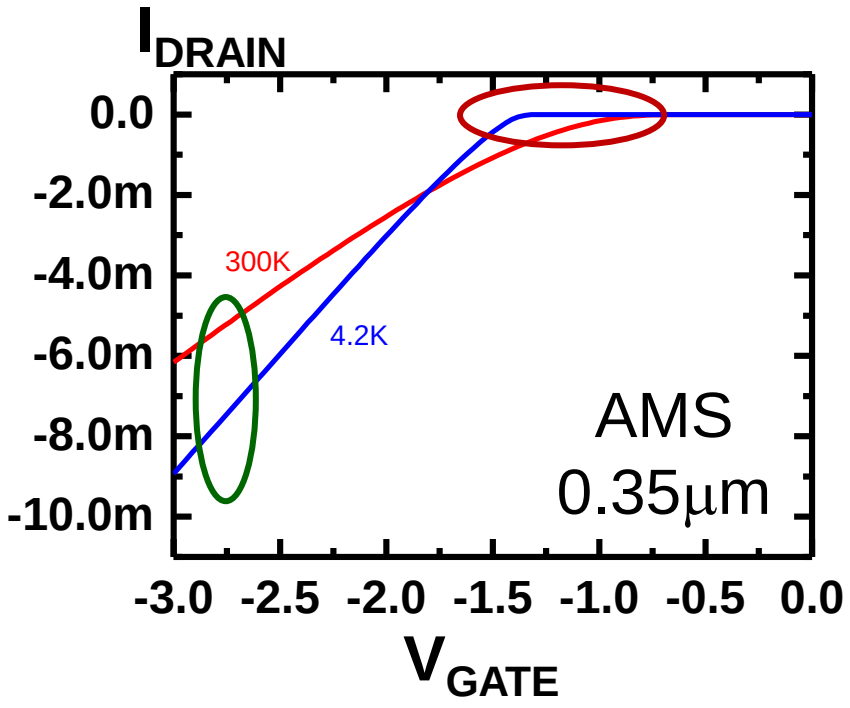


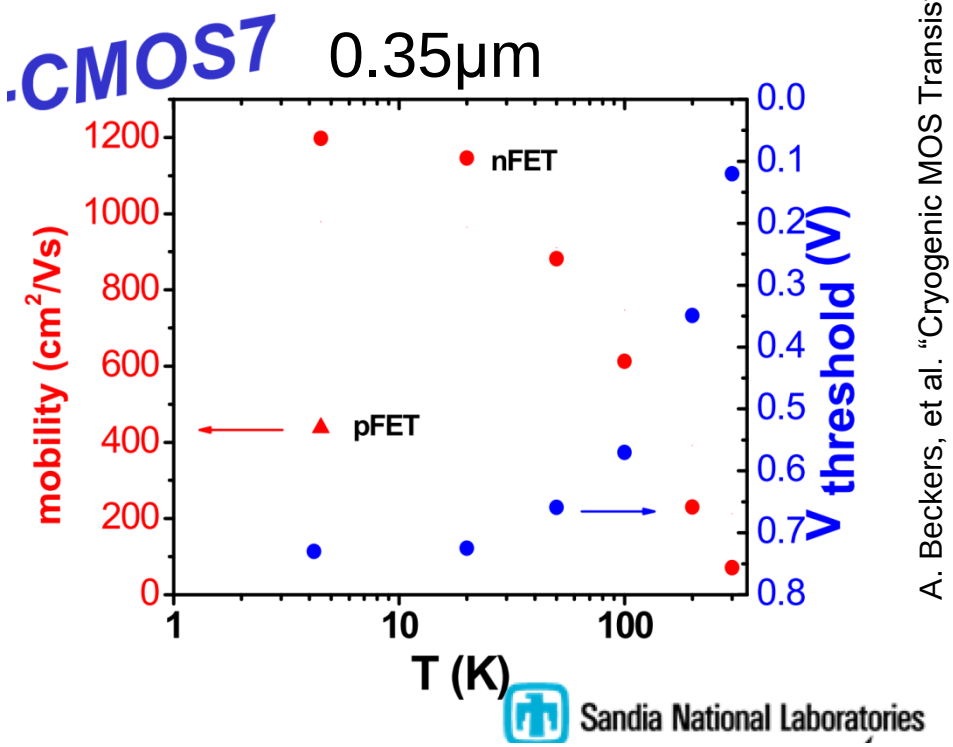
very similar to the room temperature behavior!

Effects of low temperature

- reduction in electron - phonon scattering
  → increase in carrier mobility

- substrate Fermi level shifts near to E_C (pMOS)
  → increase of the threshold voltage



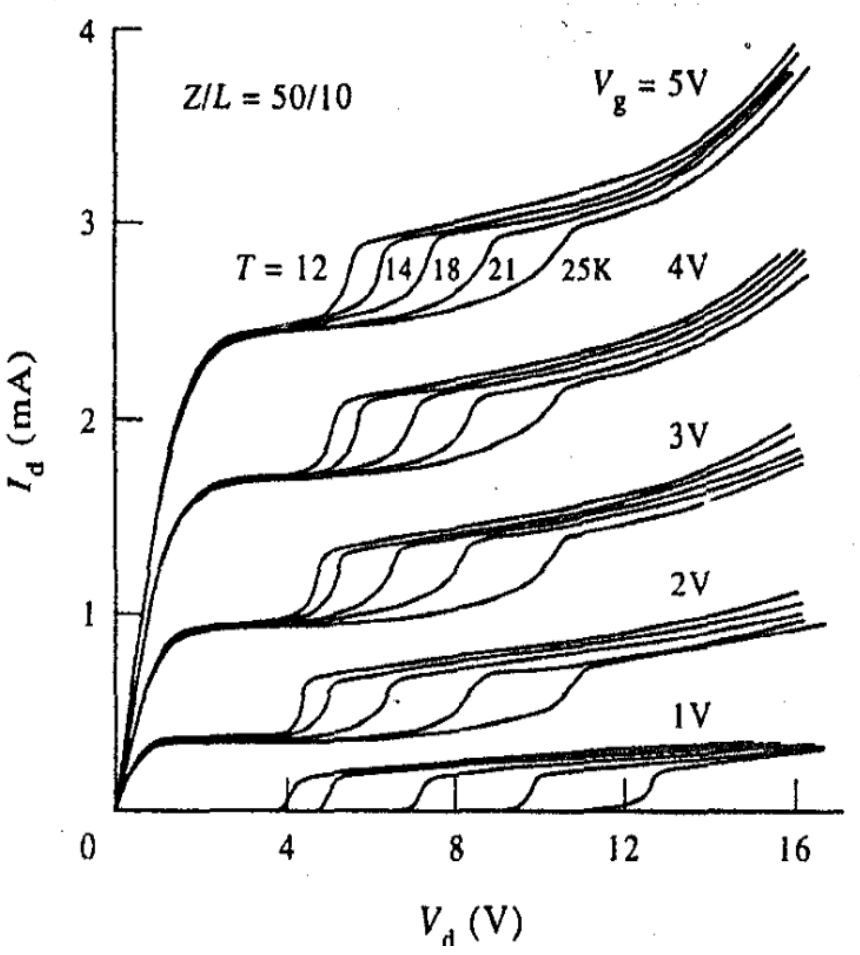


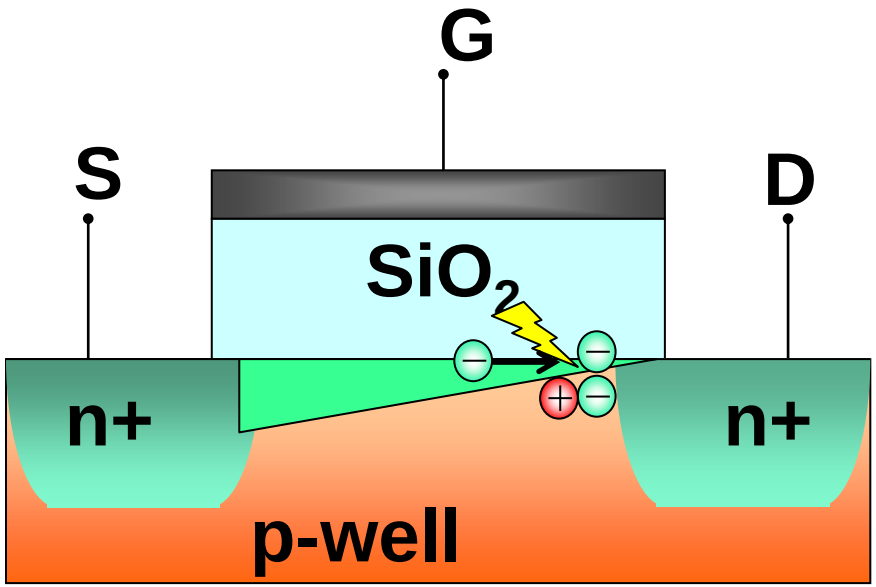
A. Beckers, et al. "Cryogenic MOS Transistor Model," *IEEE TED*, 2018.

Eng et al. Silicon Qubit Workshop '09

MOSFET operating at 4K: problems

kink effect

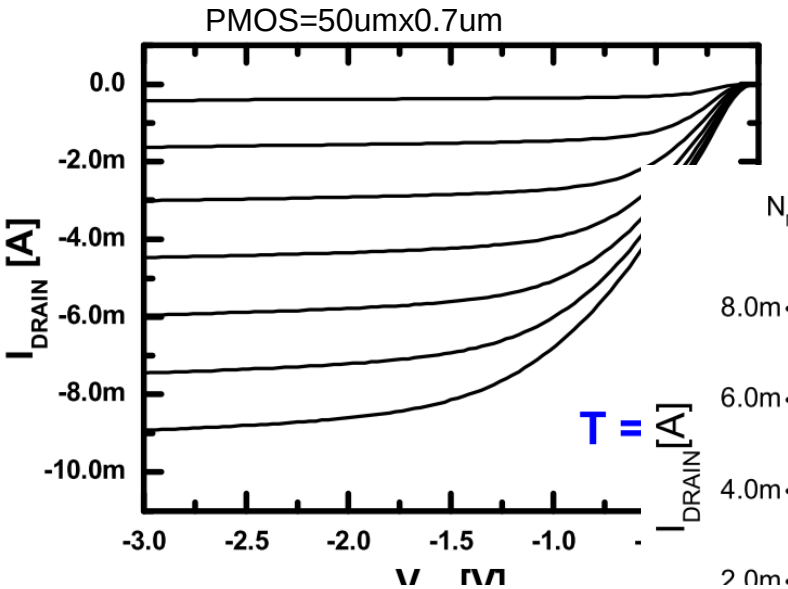




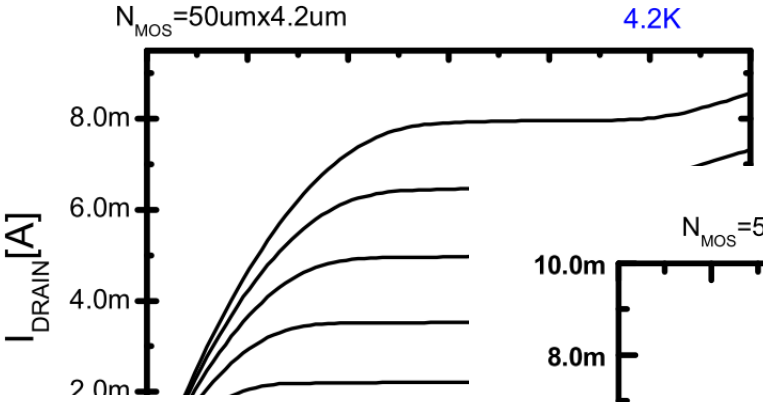
impact ionization → accumulation of holes in the frozen bulk → substrate potential increases → V_T decreases → current increases

Ghibaudo, Balestra, “Low Temperature characterization of Silicon CMOS Devices”, 1995

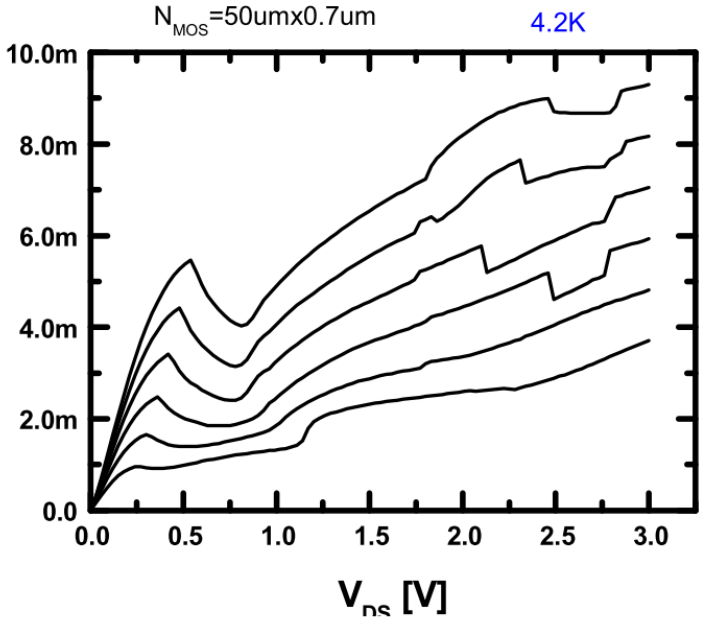
Problems are tech and size dependent

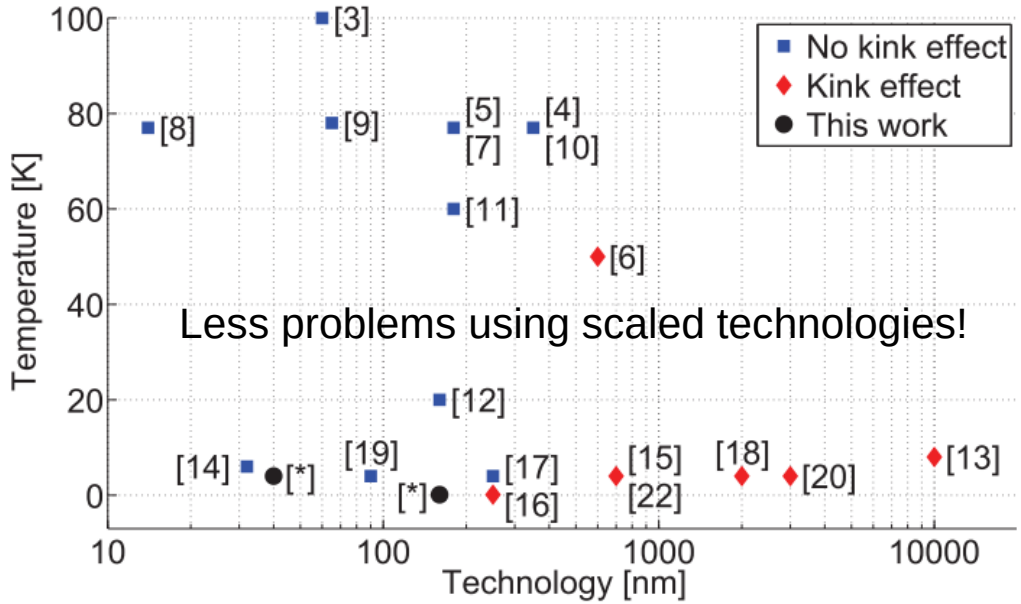


…and no models from the CMOS foundry!



AMS 0.35µm



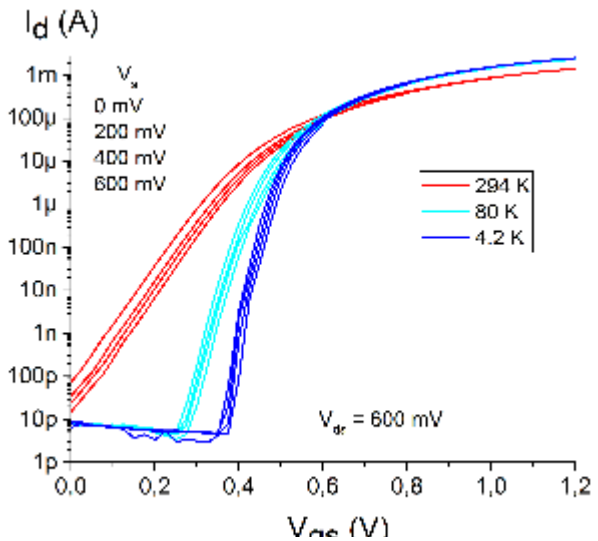


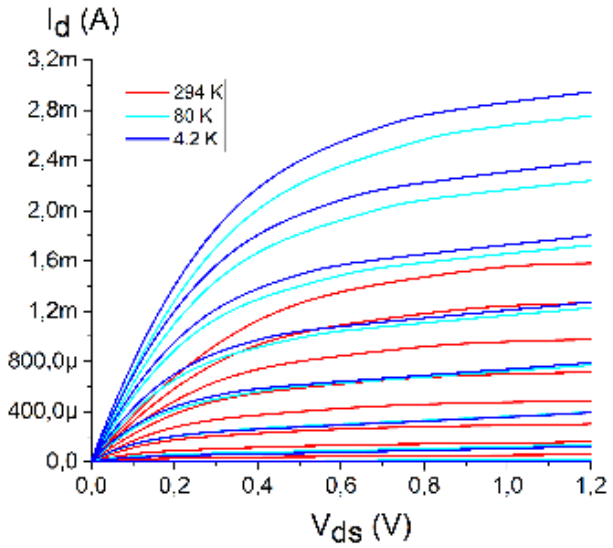
R. M. Incandela, et al.,pp. 58–61, 2017 ESSDERC.

Quantum effects in small size MOSFETs!

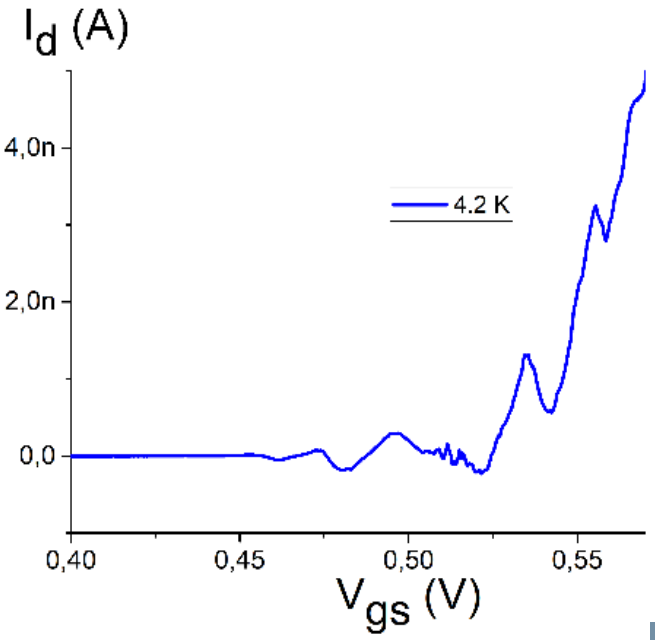
110nm CMOS

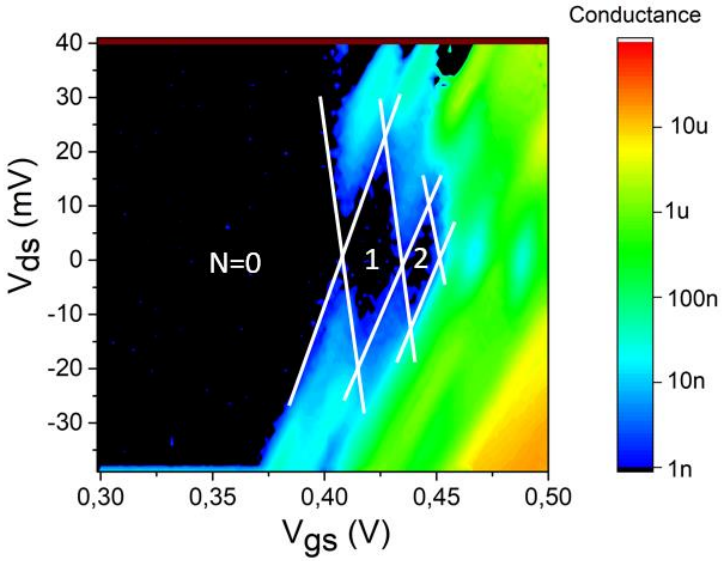
$\frac{W}{L} = \frac{10\mu m}{0.5\mu m}$





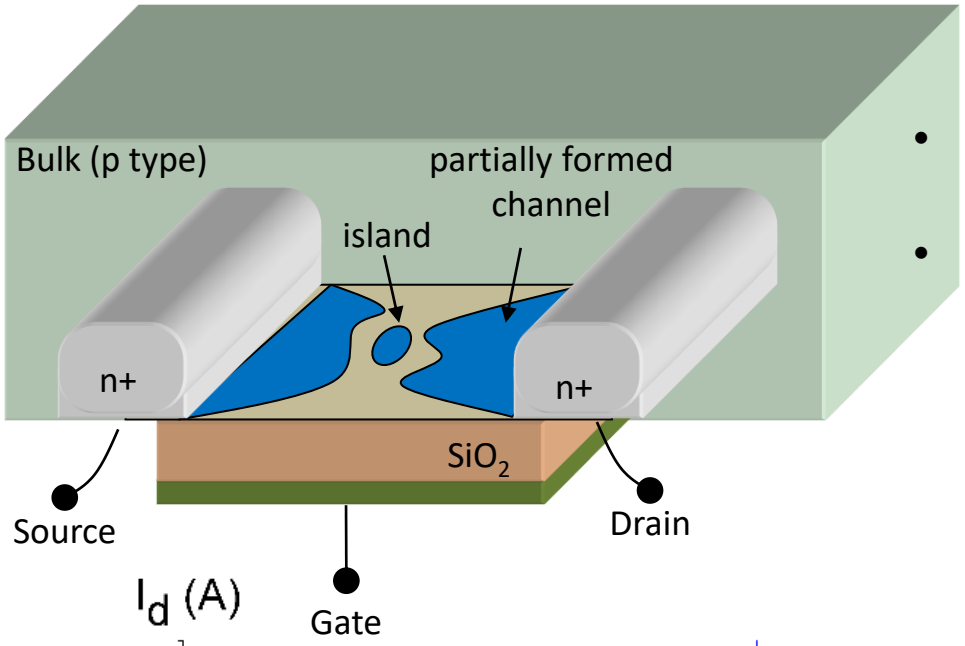
$\frac{W}{L} = \frac{140nm}{100nm}$



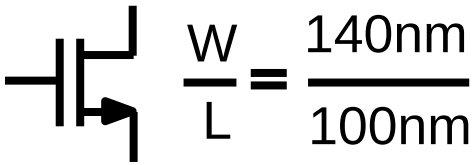


Quantum effects in small size MOSFETs!

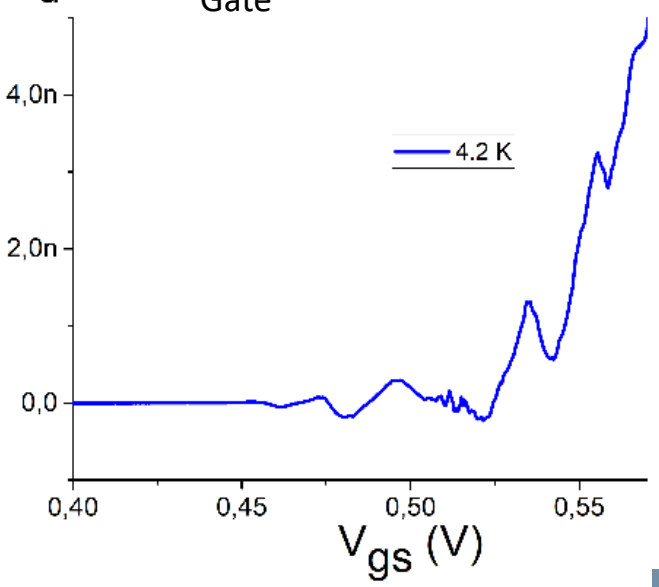
110nm CMOS

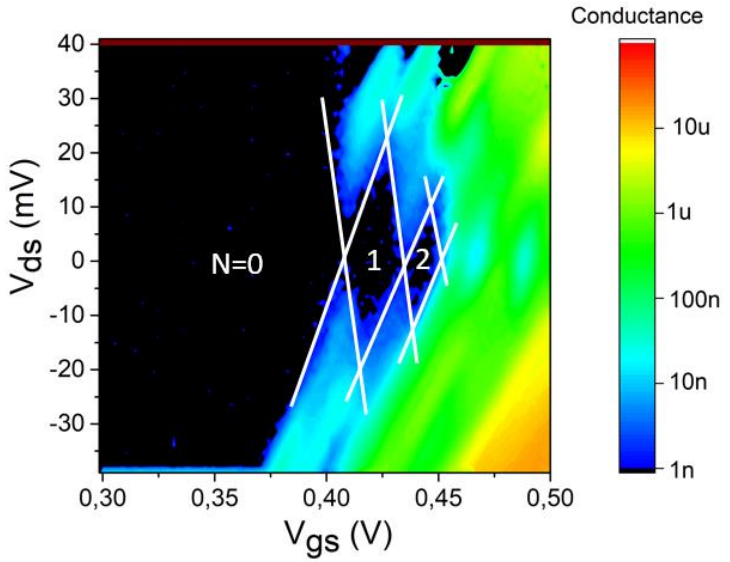


- disorder at the Si/SiO2 interface at $V_G \approx V_T$
- donor atoms can be randomly diffused in the channel region



$$\frac{W}{L} = \frac{140nm}{100nm}$$





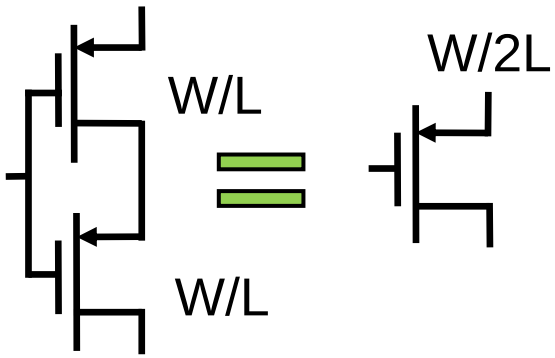
Design rule 1: characterize the technology!

MOS parameters strongly depend on the size and tech

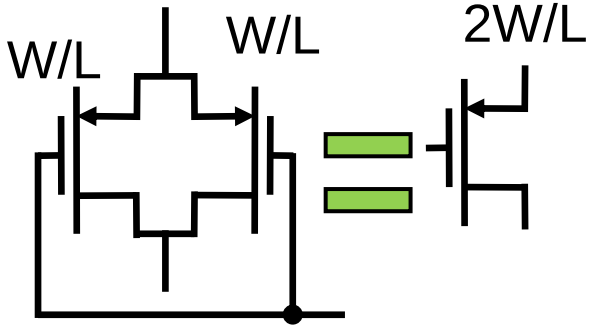
Experimental characterization of YOUR technology is MANDATORY

For simple circuits 1 nMOS and 1 pMOS is enough

series or parallel combinations of these basic transistors

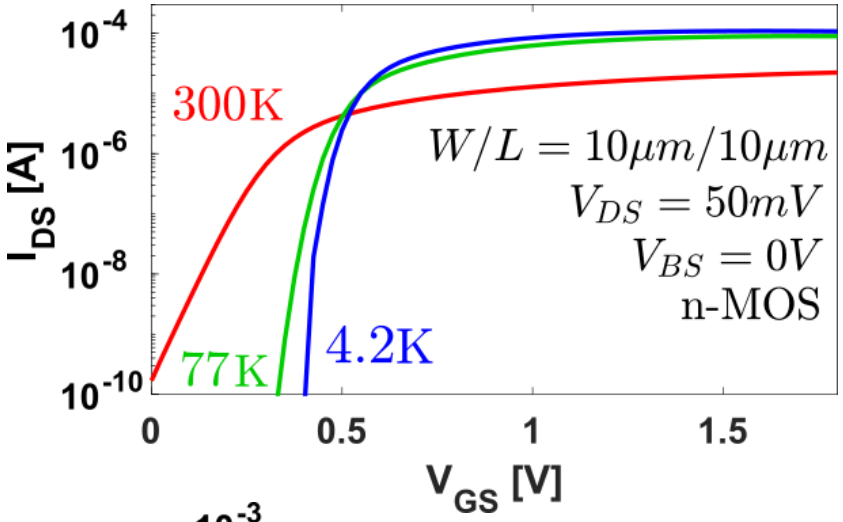


less conductive MOS

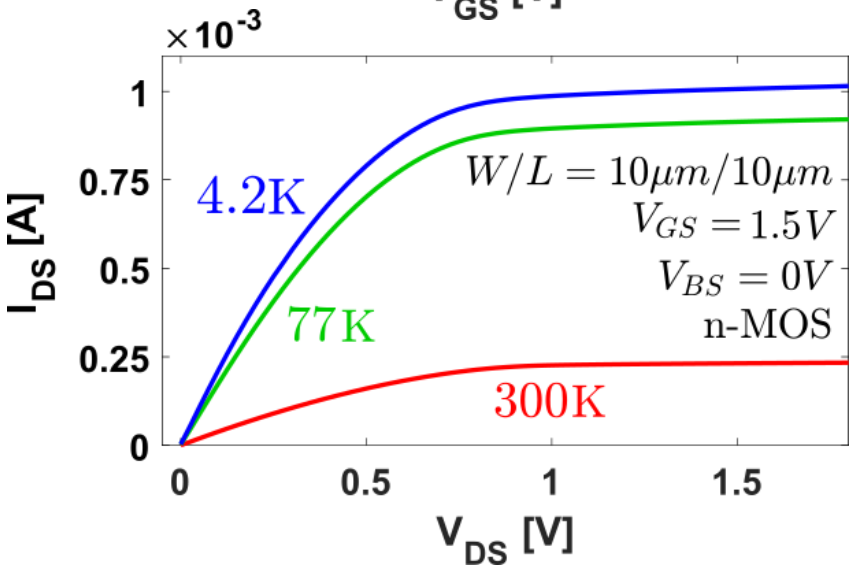


more conductive MOS

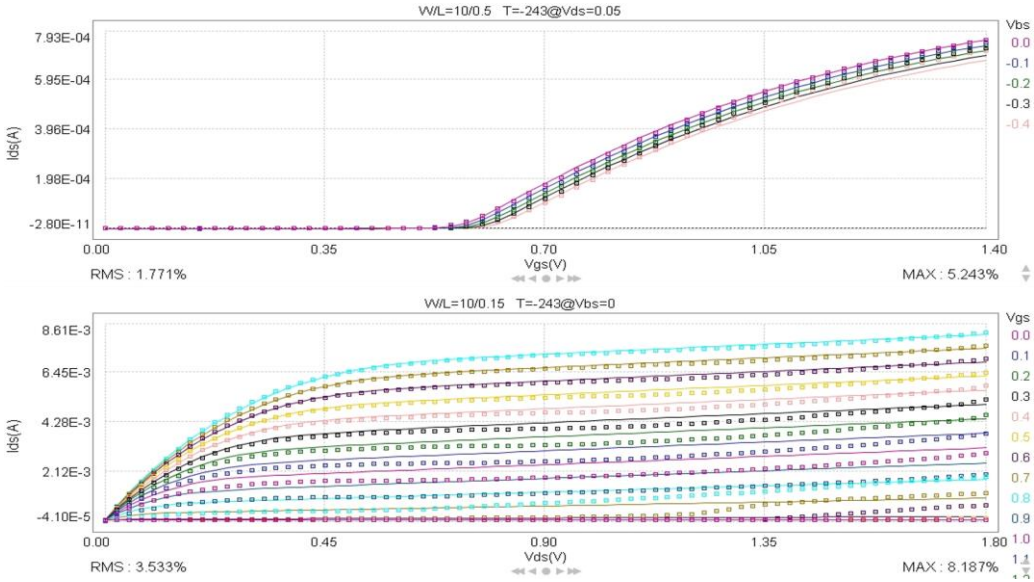
150nm CMOS technology – DC characterization



	RT	4.2K	Δ%
V_{Th}	$0{,}4V$	$0{,}56V$	$+40\%$
μ_0	$300\frac{cm^2}{Vs}$	$900\frac{cm^2}{Vs}$	$+200\%$
STS	$70\frac{mV}{dec}$	$7\frac{mV}{dec}$	-90%



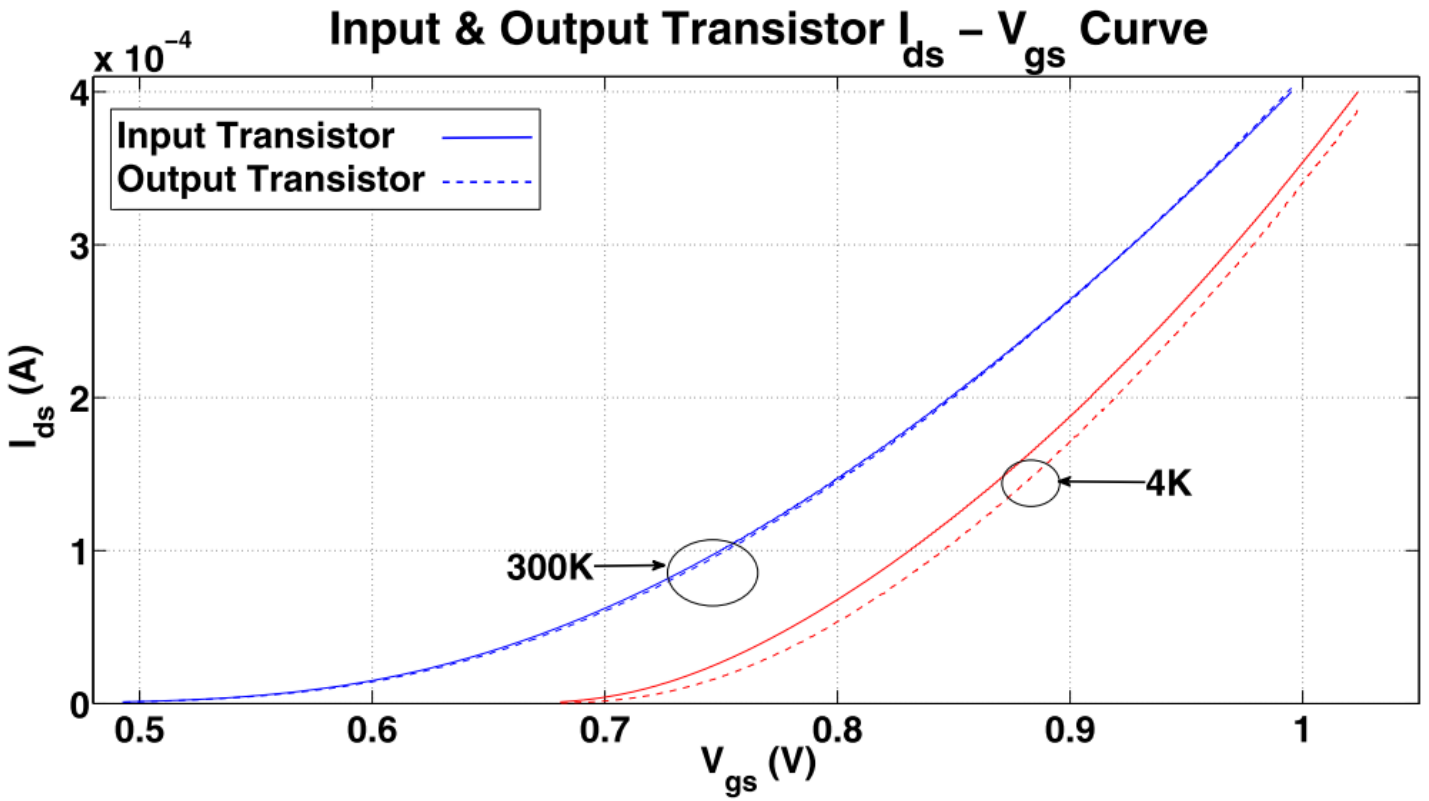
Standard BSIM models are accurate enough:



❑ n-MOS $err_{MAX} \approx 15\%$ $(peak\ 23\%)$

❑ p-MOS $err_{MAX} \approx 18\%$ $(peak\ 32\%)$

Design rule 2: pay attention to mismatch!

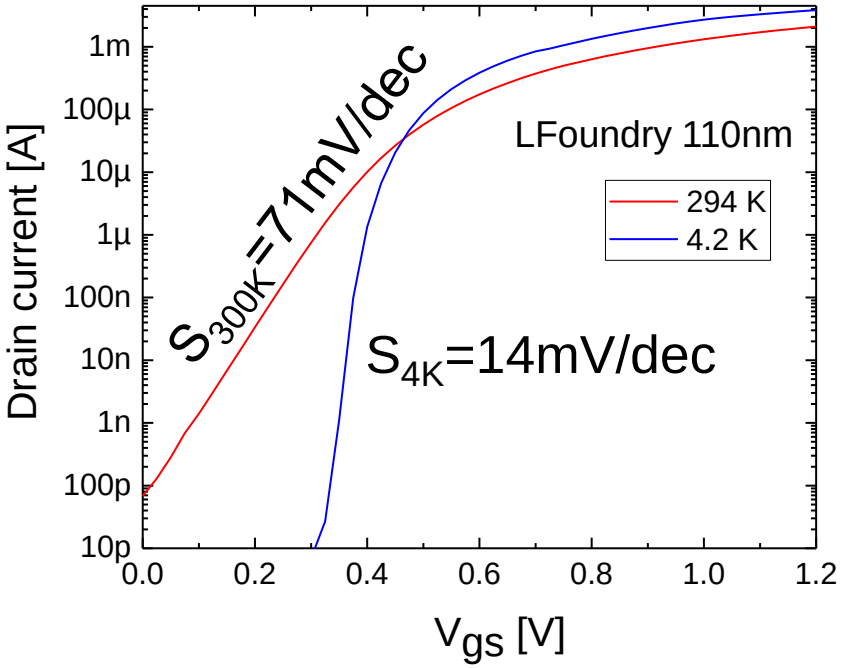


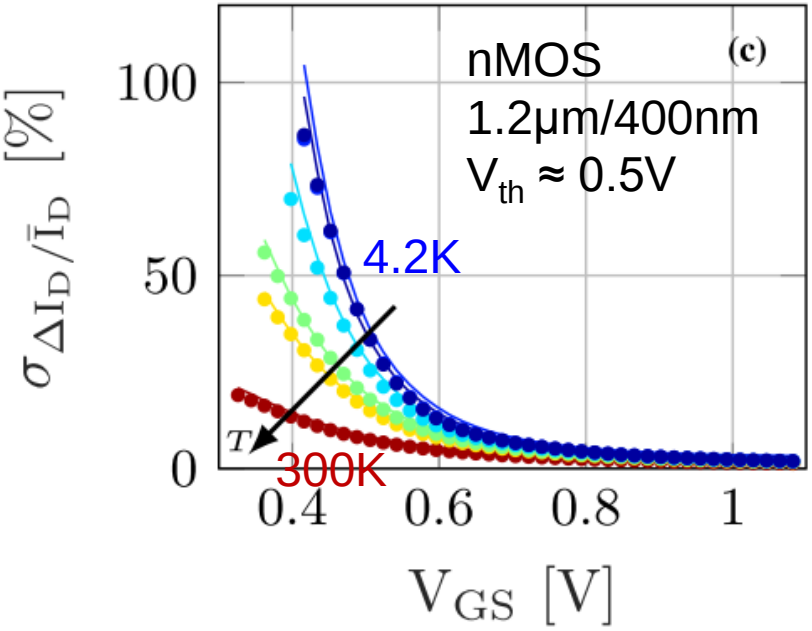
K. Das et al. EEE Symposium on Circuits and Systems, 2010

worsening of mismatch by a factor of 1.5-3 at low temperature compared to room temperature (tech dependent).

➡ Degradation of the offset voltage, linearity of ADC, DAC, bias setting

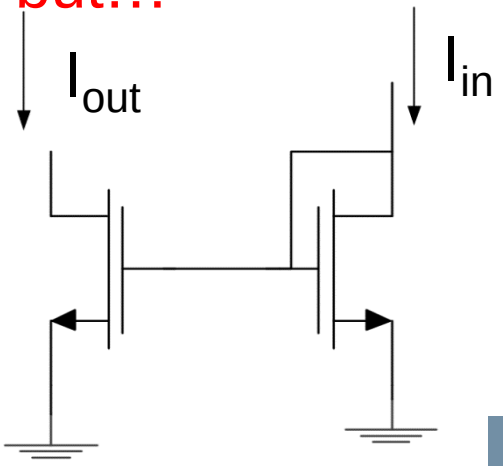
Design rule 3: subthreshold is critical





P. A. T'Hart, et al. *IEEE J. Electron Devices Soc.*, pp. 263–273, 2020

Higher g_m and I_{on}/I_{off}, good! but…



V_T mismatch of 5mV:

$$I_{out,300K} \approx I_{in}\, 10^{\frac{5mV}{S_{300K}}} = I_{in} \cdot 1.17$$

$$I_{out,4K} \approx I_{in}\, 10^{\frac{5mV}{S_{4K}}} = I_{in} \cdot 2.28$$

Design rule 4: dynamic range

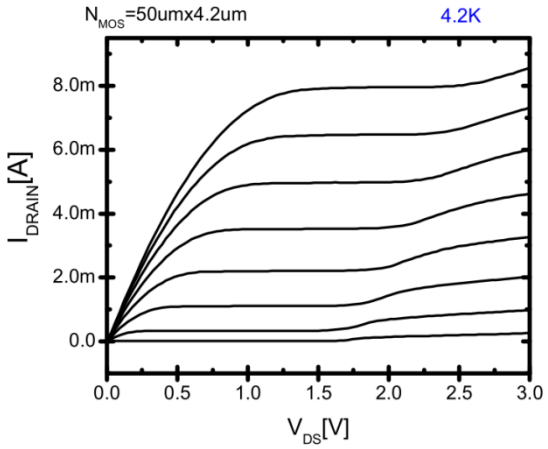
AMS 0.35µm: parameters from 300K to 4K

- $V_{T,n}$ from 0.45V to 0.7V
- $V_{T,p}$ from -0.7V to -1.4V
- Power supply: still 3.3V
- no subthreshold

stack up few transistors!

and

kink effect



limit the V_{DS}!

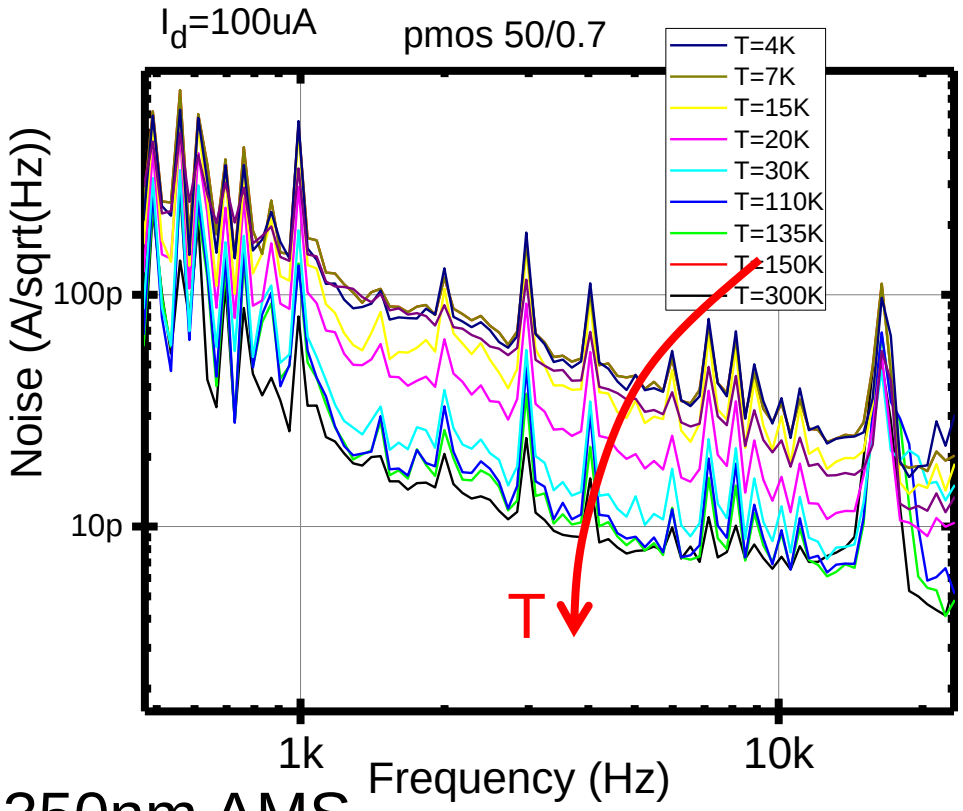
Noise

Thermal noise: $\overline{e_n^2} = 4kT\frac{\gamma}{g_m}$

T ↘ , g_m ↗ → ***noise ↘ ↘***

(0.1nV/ √Hz))

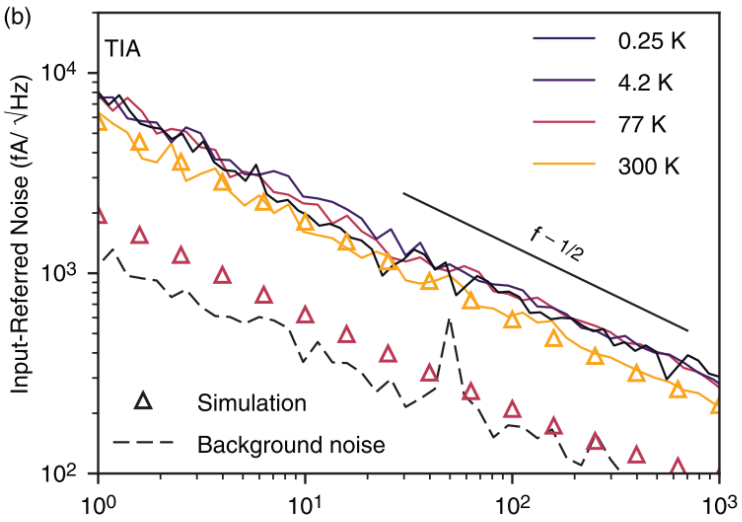
Flicker noise: usually does not decrease



350nm AMS

dominant noise up to tens of MHz

28nm FDSOI tech.



L. Le Guevel *et al.*, "Low-power transimpedance amplifier for cryogenic integration with quantum devices," *Appl. Phys. Rev.*, 2020

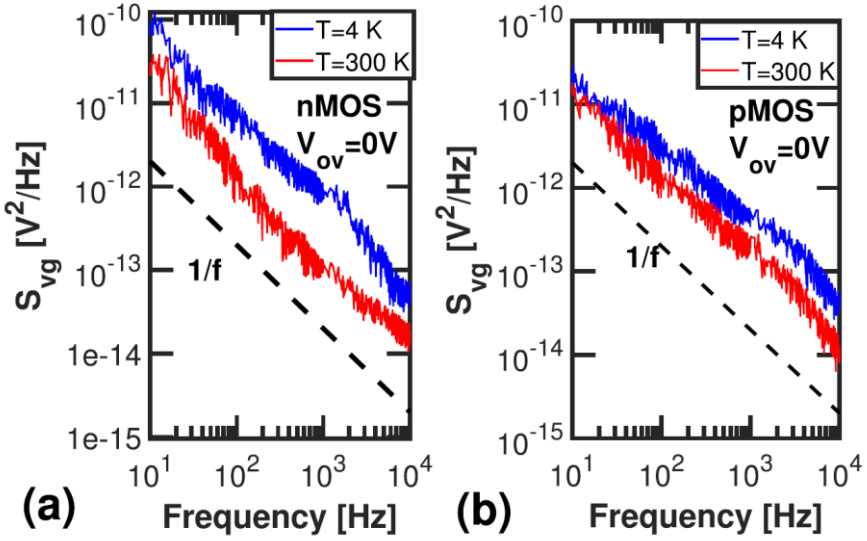
Noise

Thermal noise: $\overline{e_n^2} = 4kT\frac{\gamma}{g_m}$

T ↘ , g_m ↗ → ***noise ↘ ↘***
(0.1nV/ √Hz))

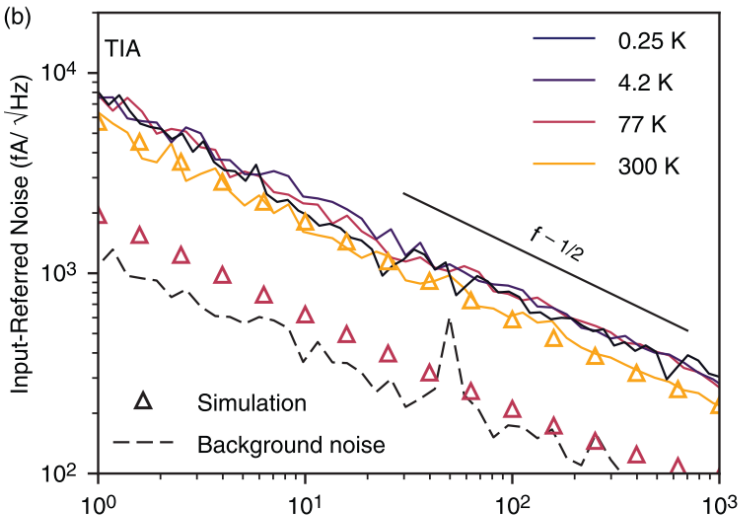
Flicker noise: usually does not decrease

28nm tech.



dominant noise up to tens of MHz

28nm FDSOI tech.



R. Asanovski, et al., "Understanding the Excess 1/f Noise in MOSFETs at Cryogenic Temperatures," *IEEE Trans. Electron Devices*, 2023

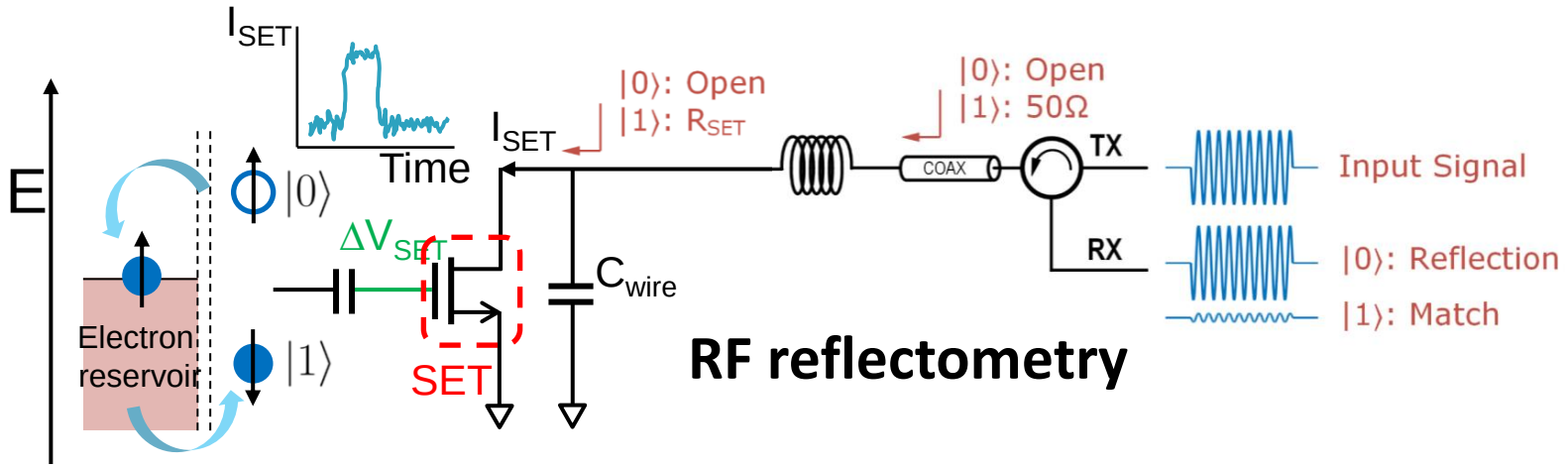
L. Le Guevel *et al.*, "Low-power transimpedance amplifier for cryogenic integration with quantum devices," *Appl. Phys. Rev.*, 2020

Outline

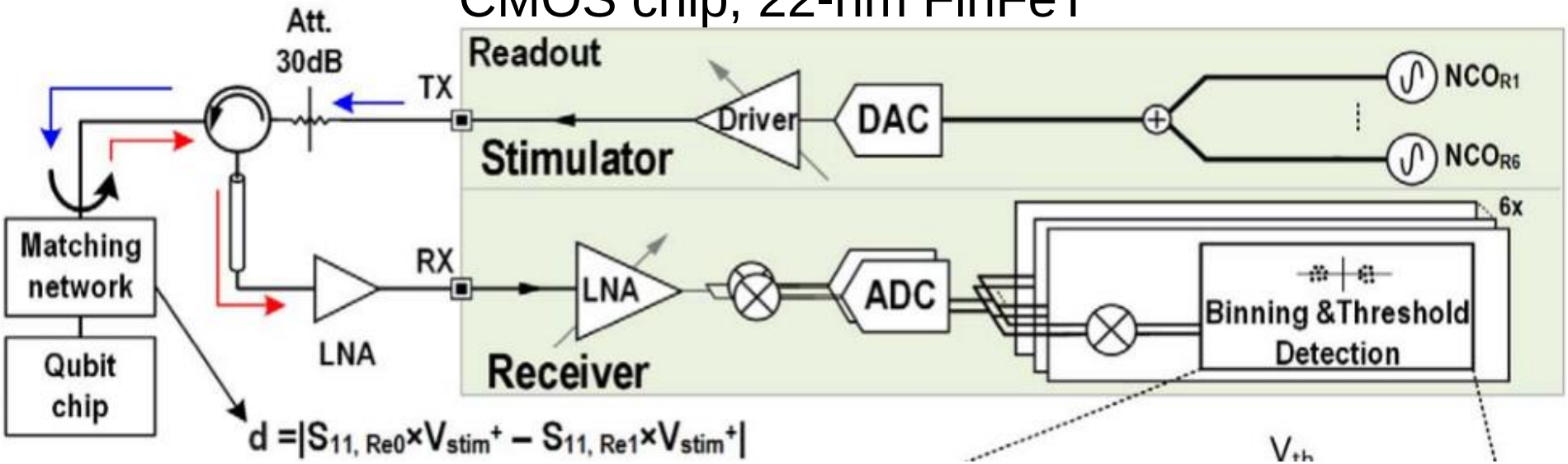
- Spin detection using room temperature instrumentation
- Cryogenic electronics
  - Challenges
  - Design rules
- Examples

Spin qubit readout: measurement technique

[S. Subramanian, ISSCC 2023]



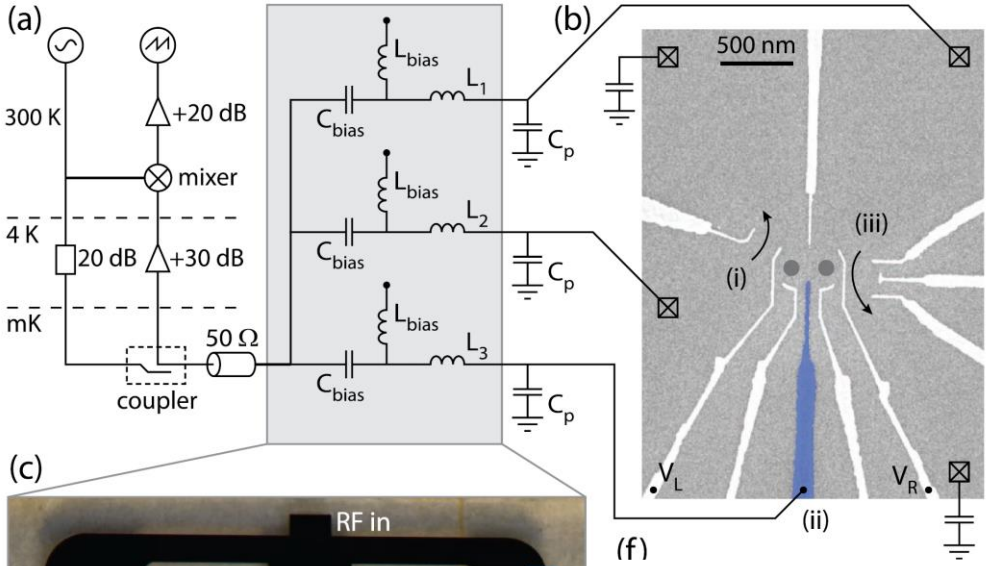
CMOS chip, 22-nm FinFeT

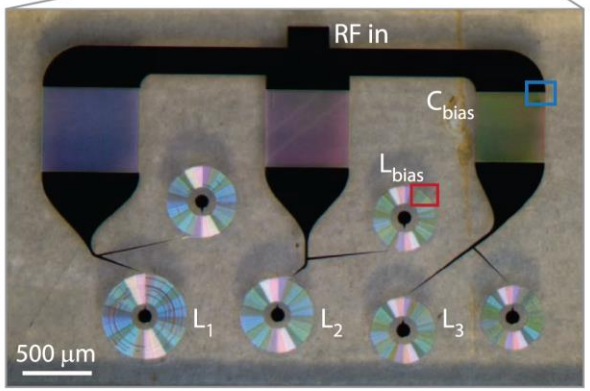


*[Park et al, "*A Fully Integrated Cryo-CMOS SoC for State Manipulation, Readout, and High-Speed Gate Pulsing of Spin Qubits",*JSSC, 2021]*

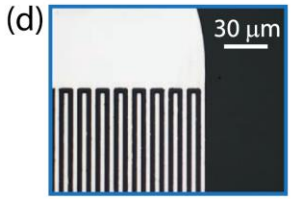
Frequency Division Multiplexing

J. M. Hornibrook et al. "Frequency multiplexing for readout of spin qubits," *Appl. Phys. Lett.*, 2014

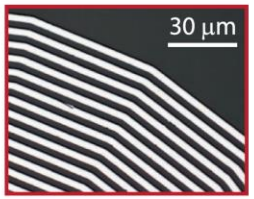




multiplexing chip superconducting niobium on a sapphire substrate (ideally, it is the same chip of the qubits)



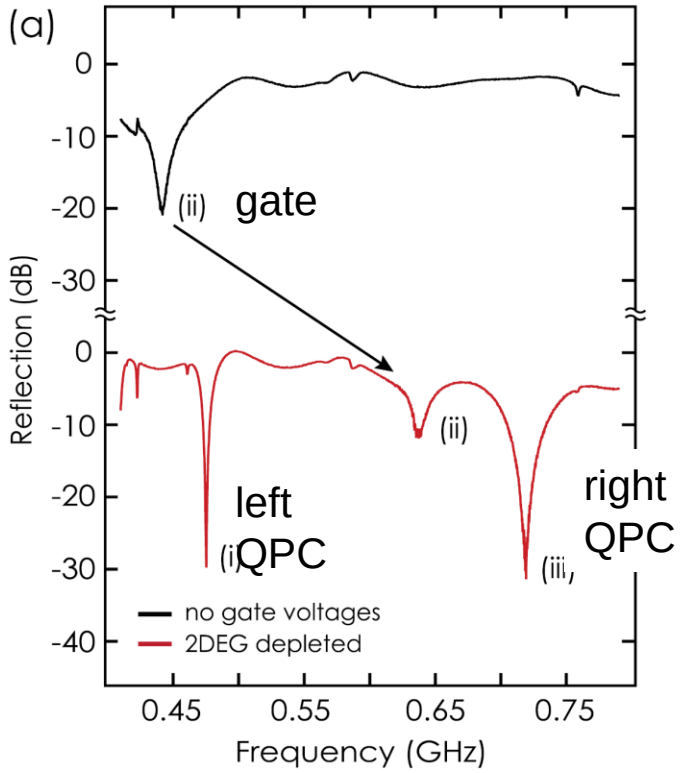
Interdigitated C



Spiral L

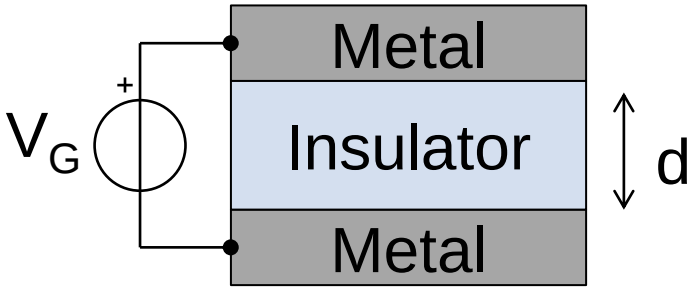
bias tees (C_{bias}, L_{bias})
2 QDs and 2 QPCs

Frequency response of MUX circuit



A single cable for many qubits

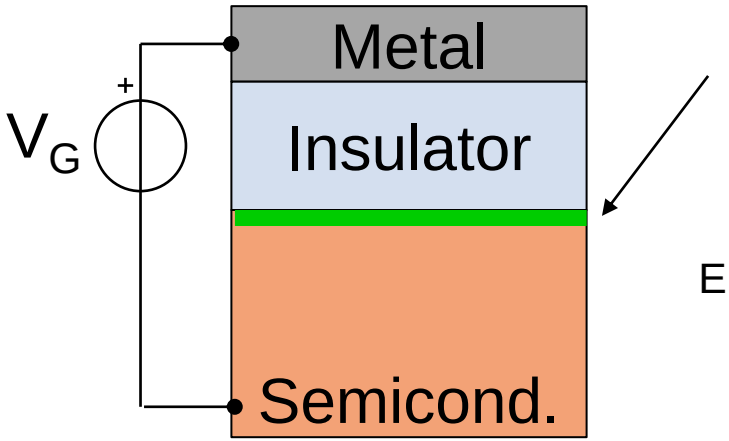
Quantum capacitance



$$\Delta Q = -q\Delta N_e = C_{geom}\Delta V_G$$

q=+1.6 10^{-19} C

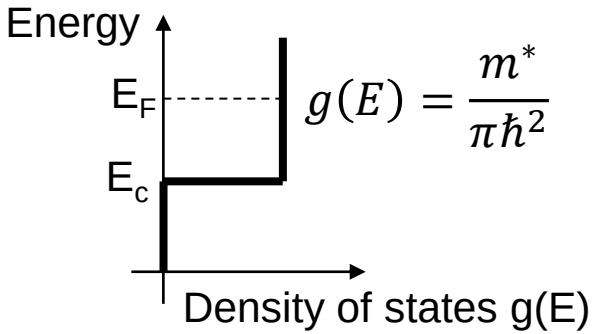
$$C_{geom} = \epsilon \frac{S}{d}$$



$V_G > V_T$

2D electron gas at potential V_c

$$\Delta Q = -q\Delta N_e = C_{geom}(\Delta V_G - \Delta V_c)$$



$$g(E) = \frac{m^*}{\pi\hbar^2}$$

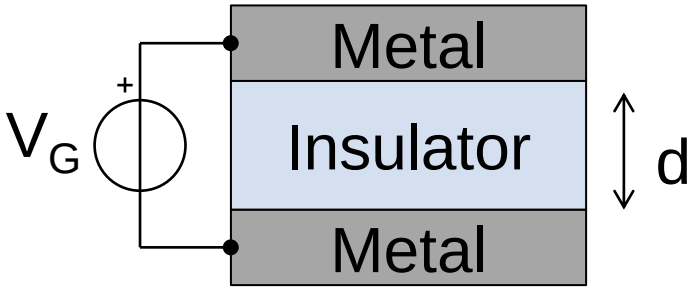
$$N_e \cong \int_{E_c}^{E_F} g(E)dE \quad (T \approx 0K)$$

$$\rightarrow \Delta N_e = -\frac{m^*}{\pi\hbar^2} q\, \Delta V_c$$

$$C_Q = \frac{m^*}{\pi\hbar^2} q^2$$

quantum capacitance

Quantum capacitance



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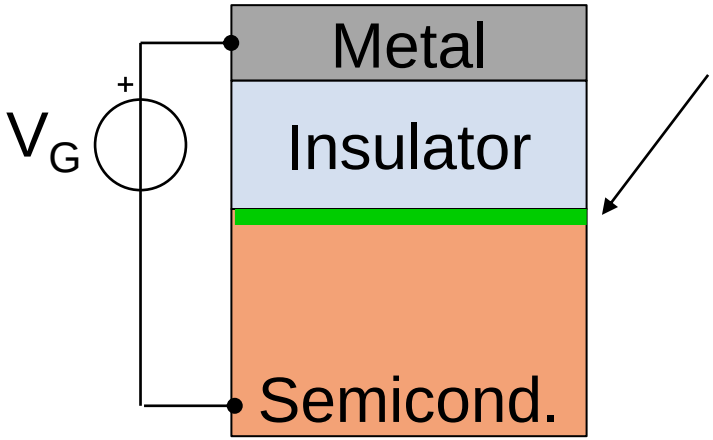
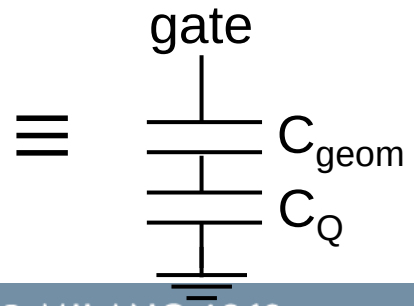


2D electron gas if $V_G > V_T$ at potential V_c

$$\Delta Q = -q\Delta N_e = C_{geom}(\Delta V_G - \Delta V_c)$$

$$-q\Delta N_e = C_{geom}\left(\Delta V_G + \frac{q\Delta N_e}{C_Q}\right)$$

$$-q\Delta N_e = \frac{C_{geom}C_Q}{C_{geom}+C_Q}\Delta V_G$$

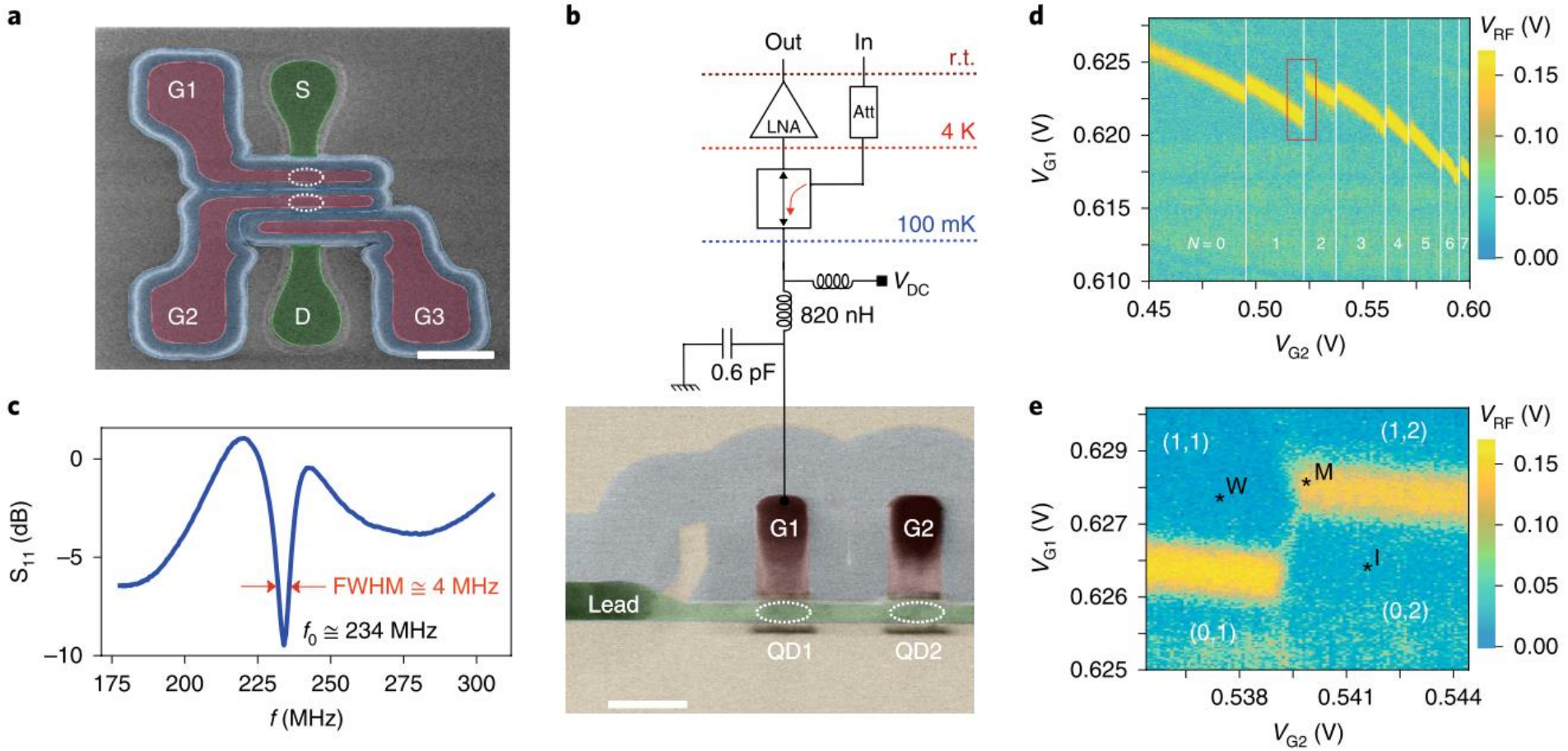


C_Q related to charge dynamics and not from geometrical parameters

$$C_Q = \frac{m^*}{\pi\hbar^2}q^2$$

quantum capacitance

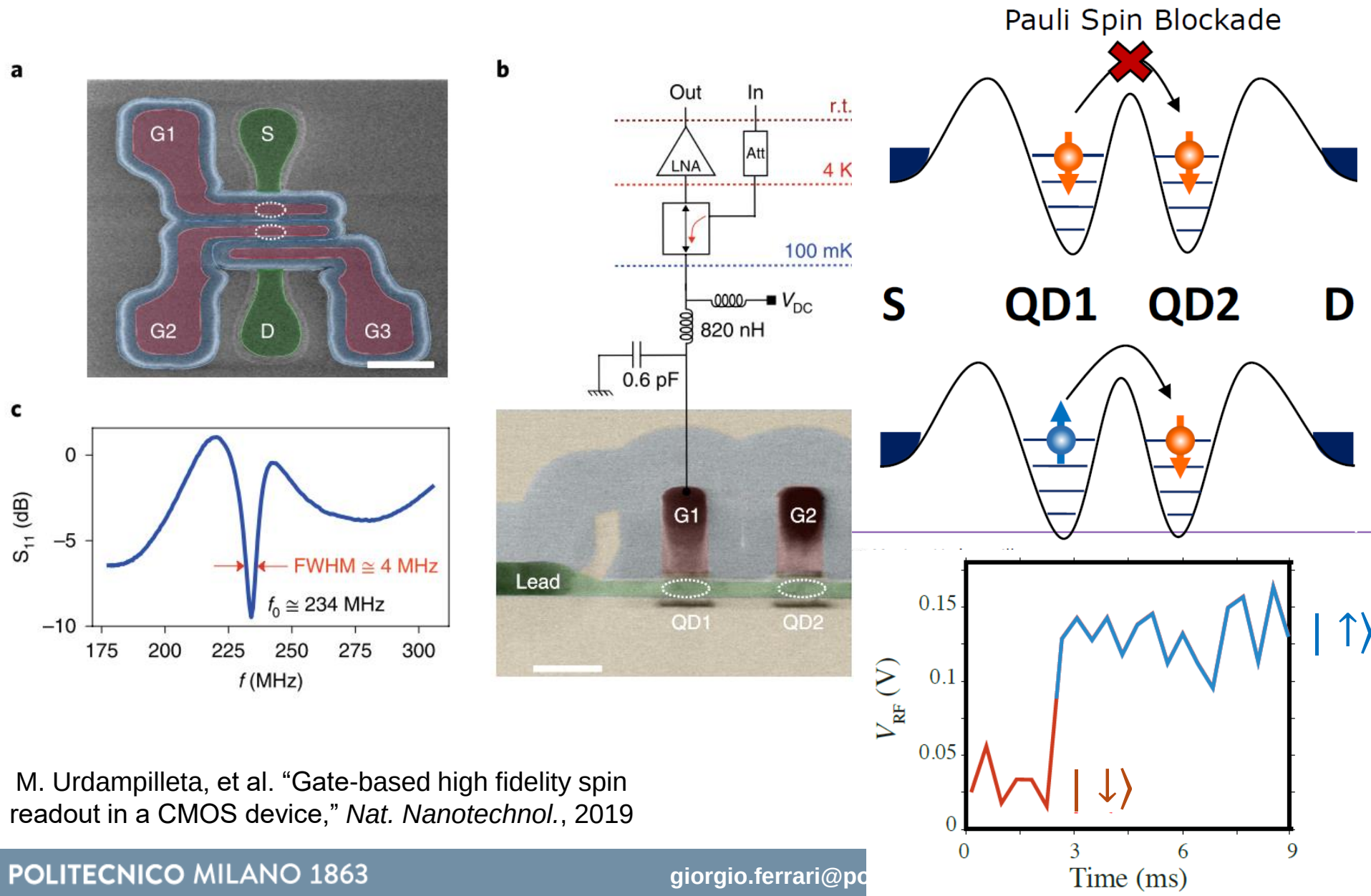
Gate-based spin readout



M. Urdampilleta, et al. “Gate-based high fidelity spin readout in a CMOS device,” *Nat. Nanotechnol.*, 2019

Gate-based spin readout

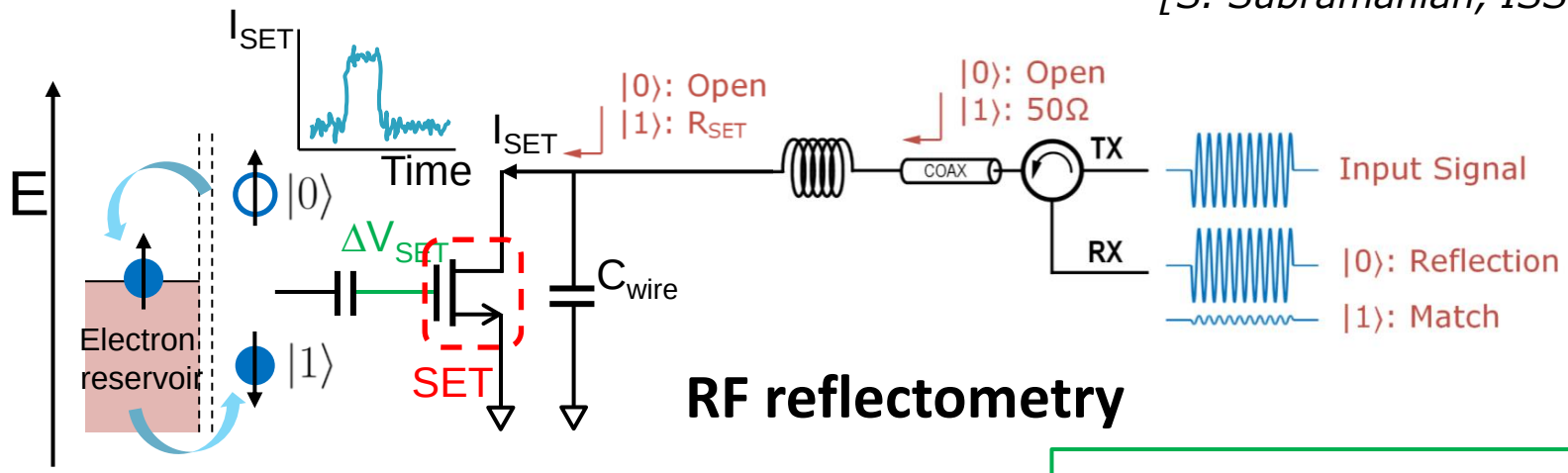
M. Urdampilleta, ESSDERC, 2020



M. Urdampilleta, et al. “Gate-based high fidelity spin readout in a CMOS device,” *Nat. Nanotechnol.*, 2019

Spin qubit readout: measurement technique

[S. Subramanian, ISSCC 2023]

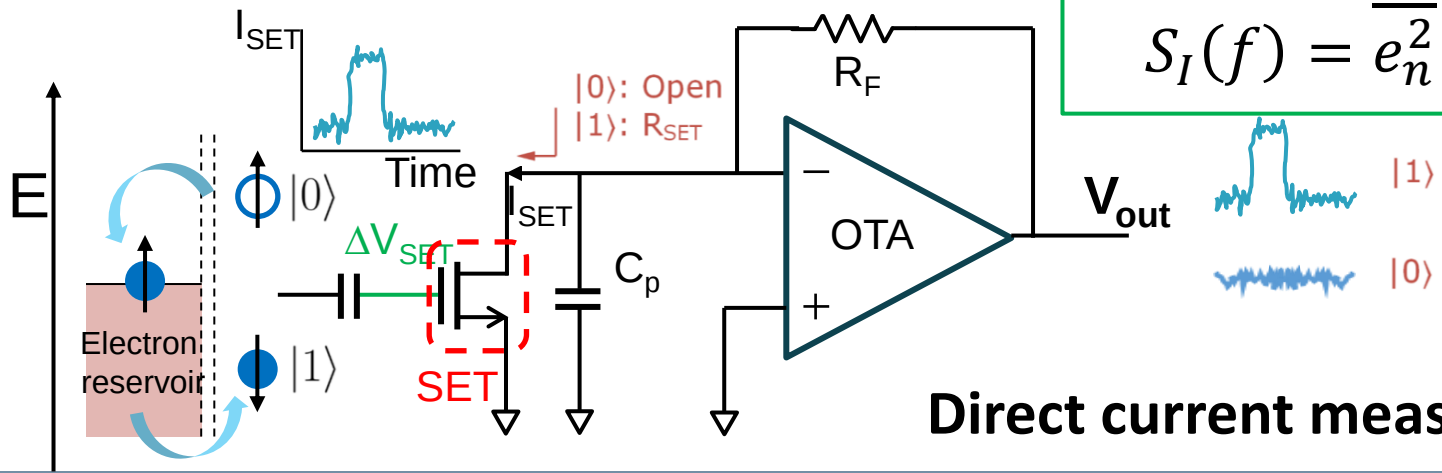


RF reflectometry

Bulky off-chip components, fast analog-to-digital converter, μ

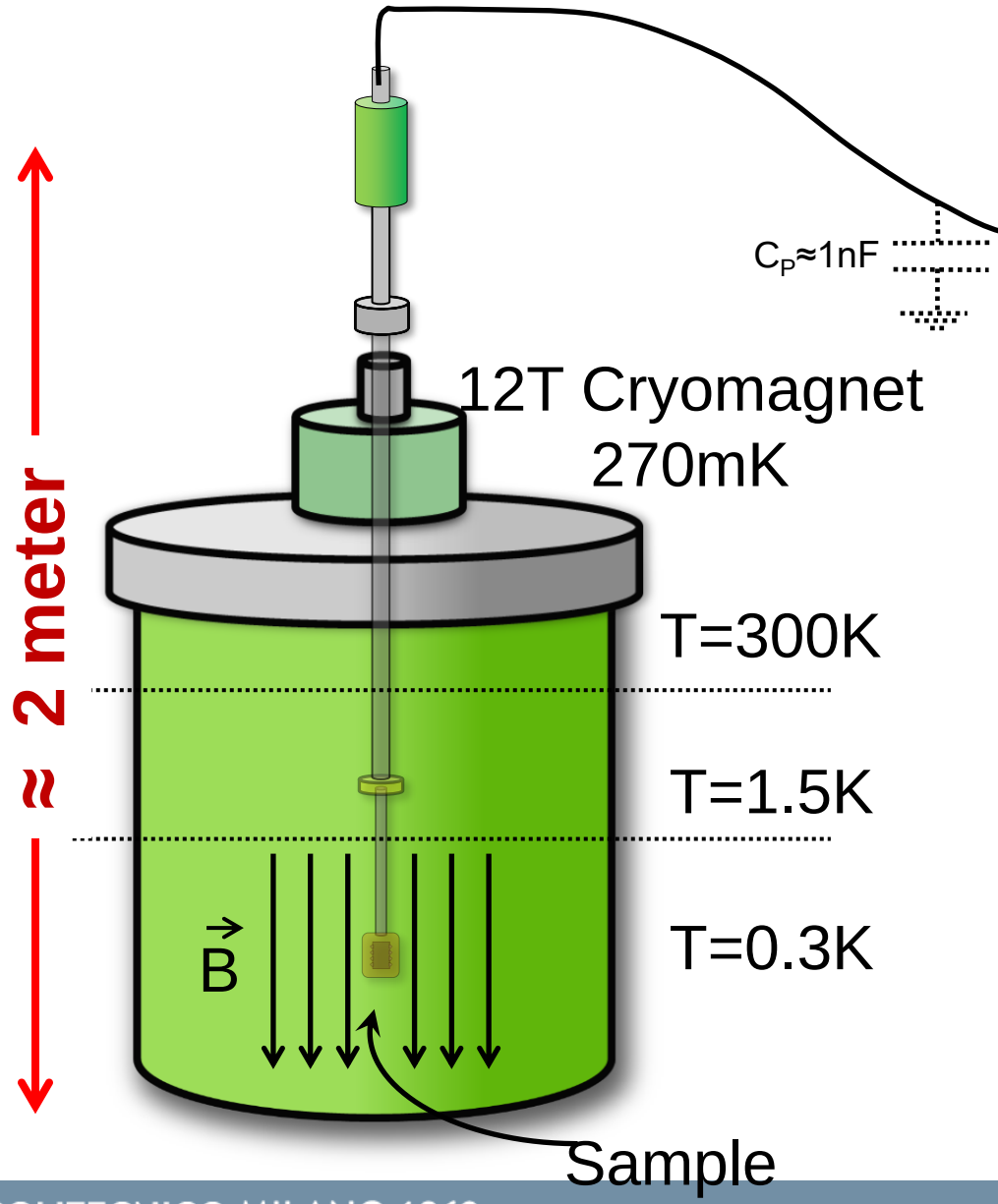
$$BW \propto \sqrt{\frac{GBWP}{C_p}}$$

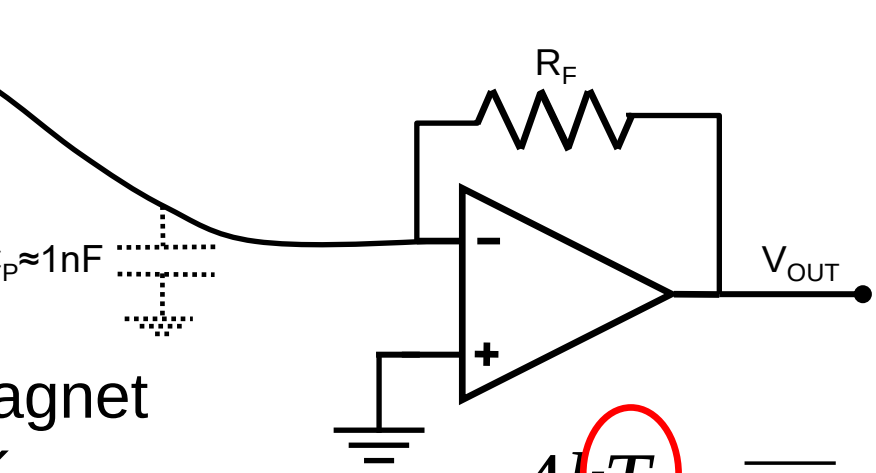
$$S_I(f) = \overline{e_n^2}(2\pi f C_p)^2$$



Direct current measurement

Cryogenic transimpedance amplifier





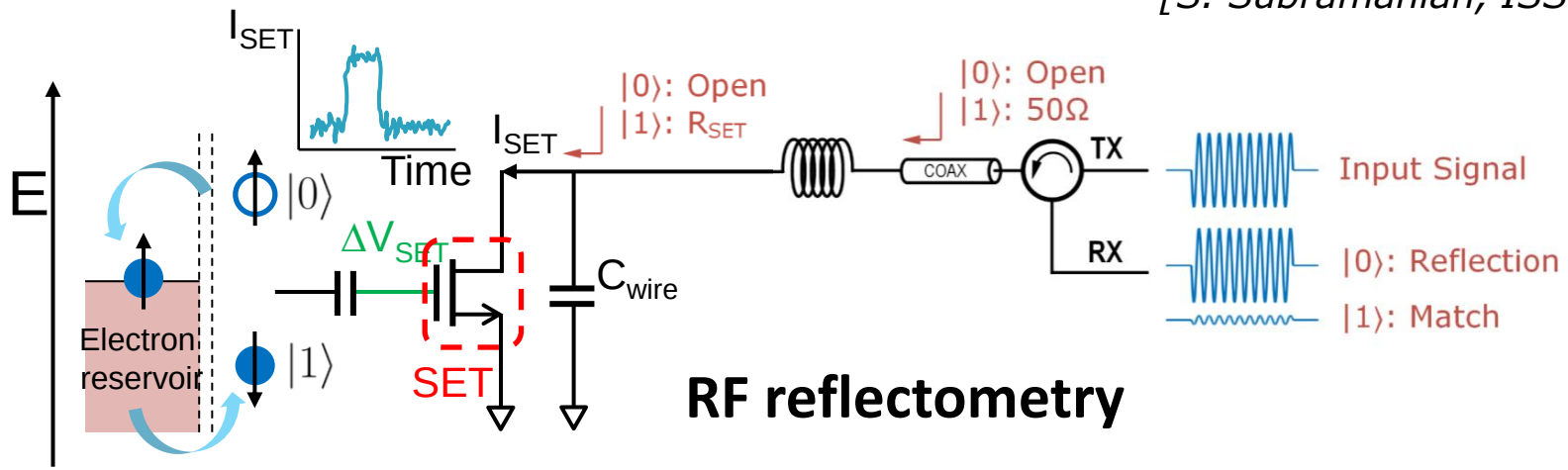
$$S_{i,eq} = \frac{4kT}{R_F} + \overline{e_N^2}\,\omega^2 C_P^2$$

Both drastically reduced

Cryo-electronics
to improve sensitivity

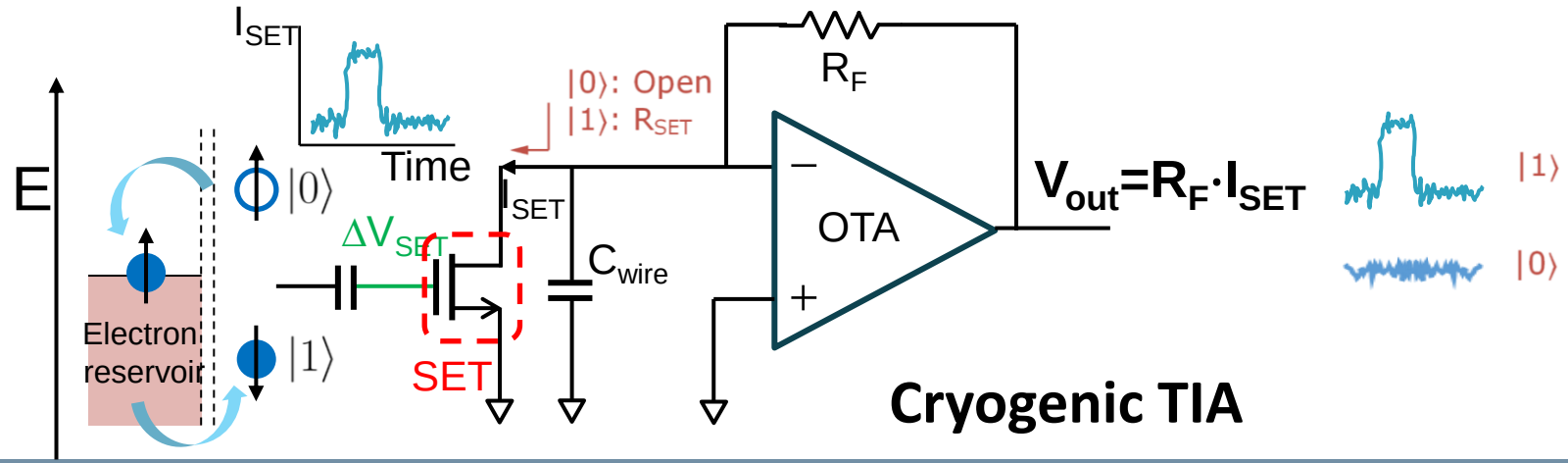
Spin qubit readout: measurement technique

[S. Subramanian, ISSCC 2023]



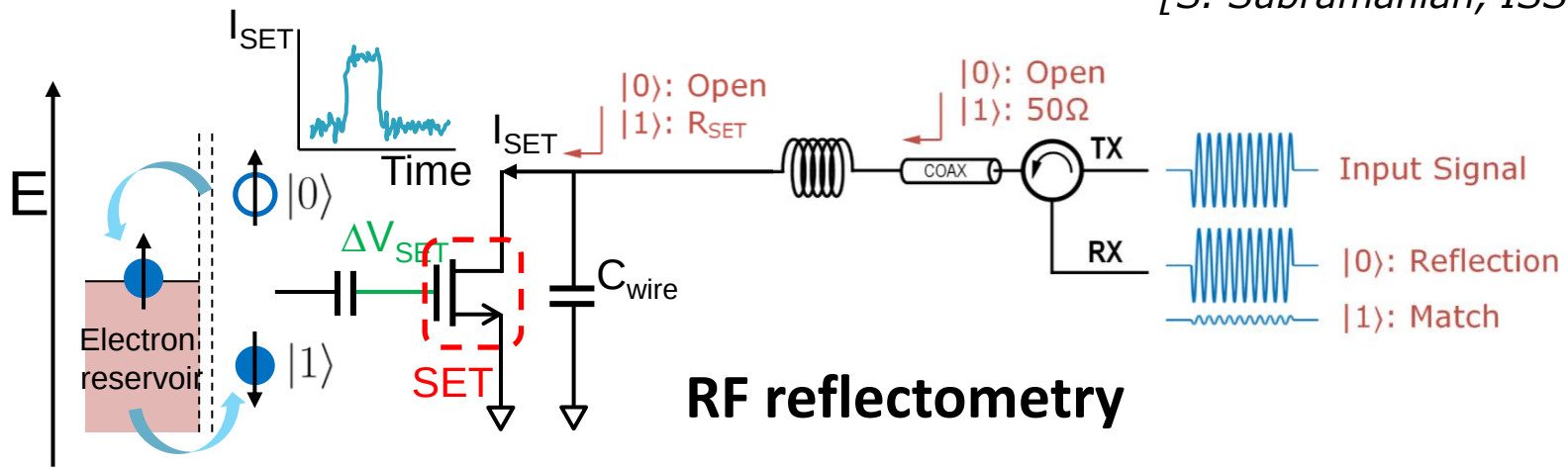
Bulky off-chip components, fast analog-to-digital converter, μ-wave signals

Fully CMOS-compatible readout operated at T<5K:



Spin qubit readout: measurement technique

[S. Subramanian, ISSCC 2023]



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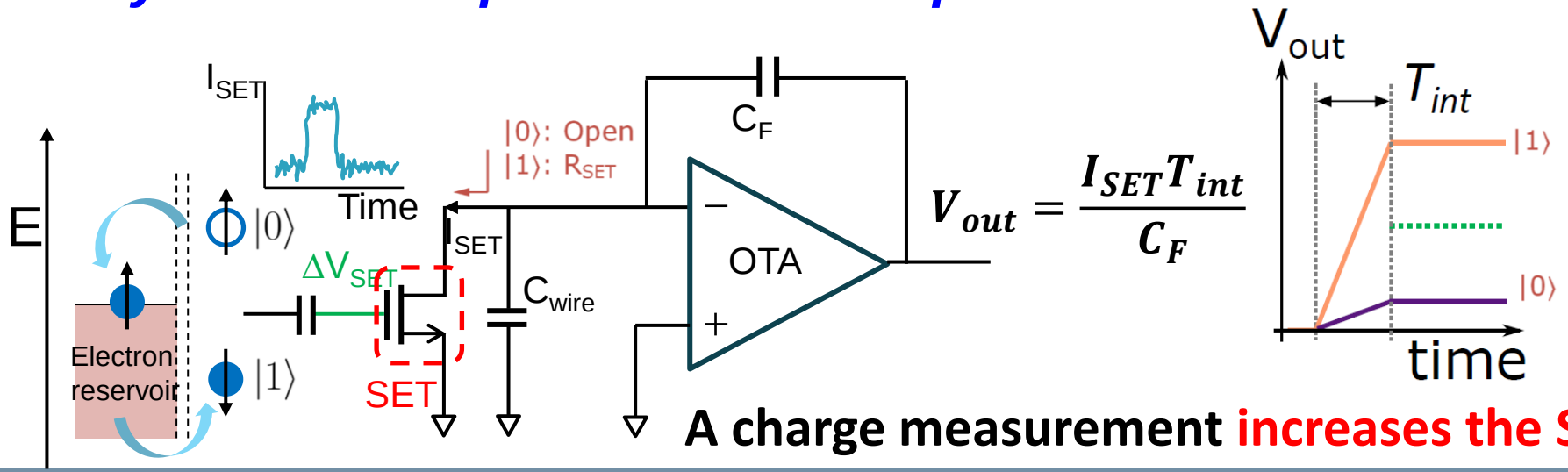
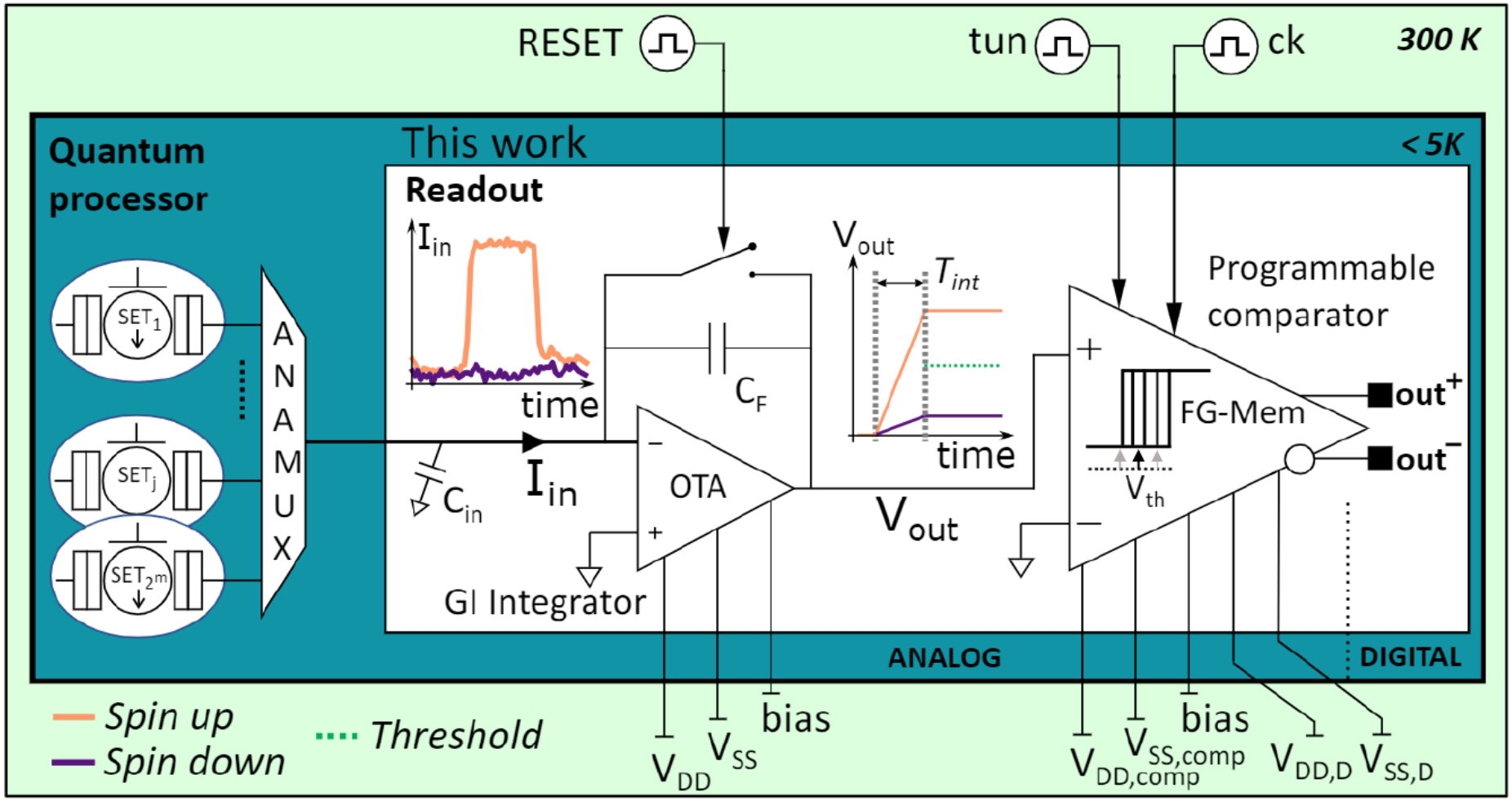


A charge measurement increases the SNR

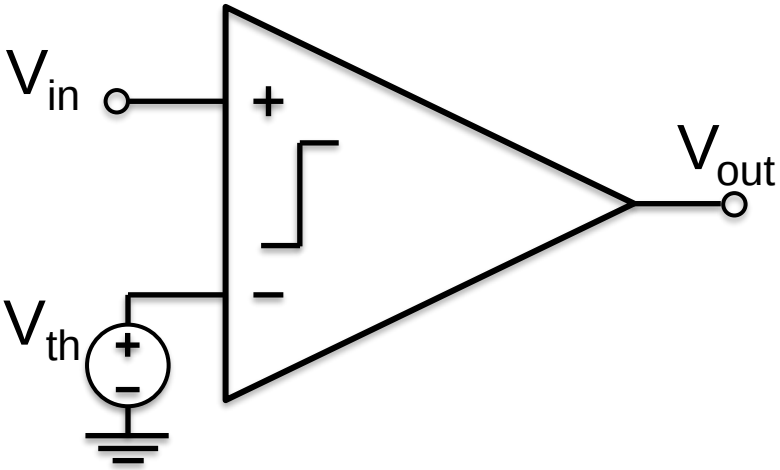
Compact readout based on current measurement

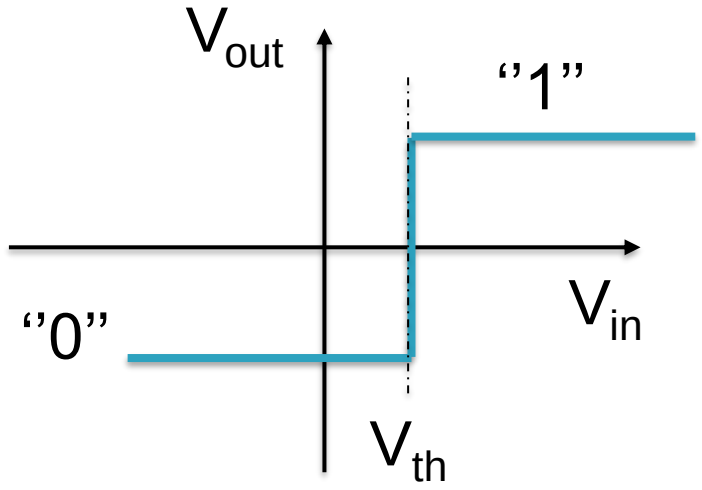


- Fully-integrated 150-nm CMOS technology
- Direct charge-to-digital conversion
- Time division multiplexing architecture
- Low power consumption (1 mW/qubit)

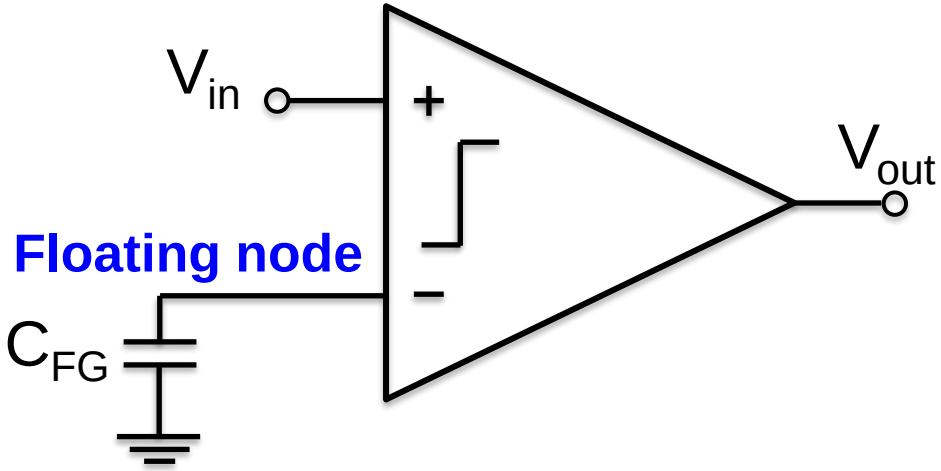
[M. CASTRIOTTA et al., IEEE *Solid-state Circuits Letters* (2023)]

Programmable floating-gate comparator





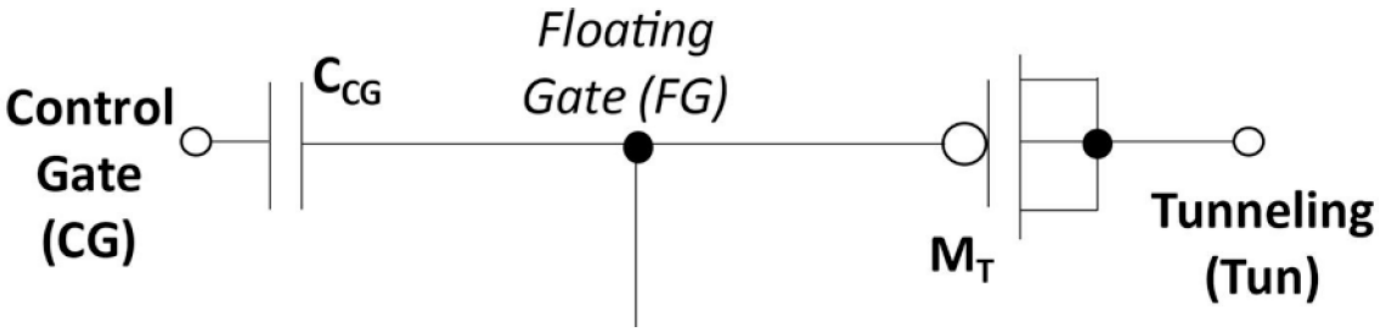
- V_{th} few mV! Process variations are critical
- Digital-to-Analog Converter (DAC): power consumption, TDMS

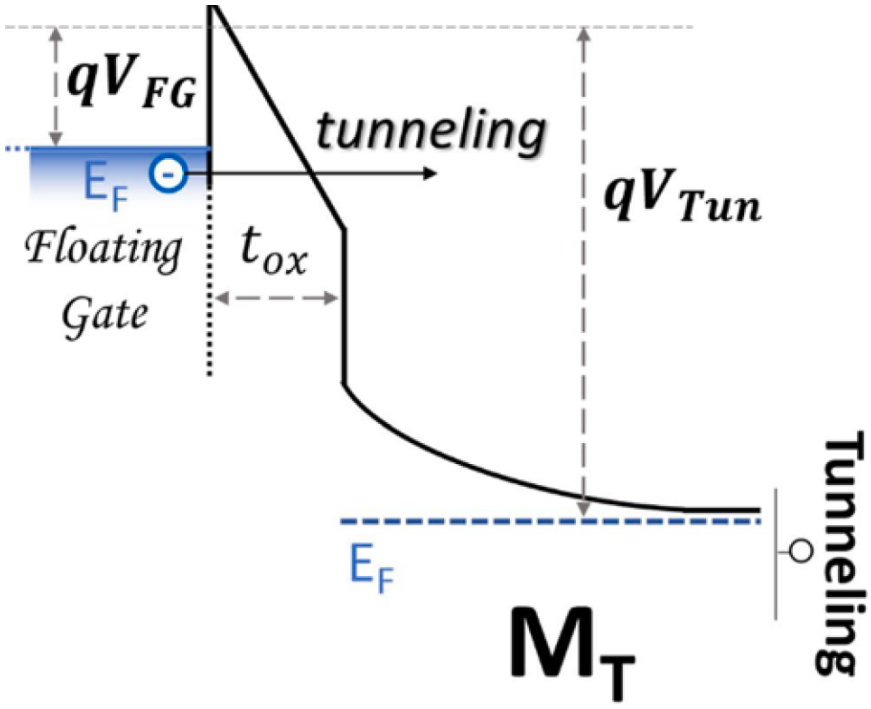


- Floating node charged at V_{th}
- Compact and low power

- How to change the charge?
- How to compensate for the process variations?

Floating gate in standard CMOS technology

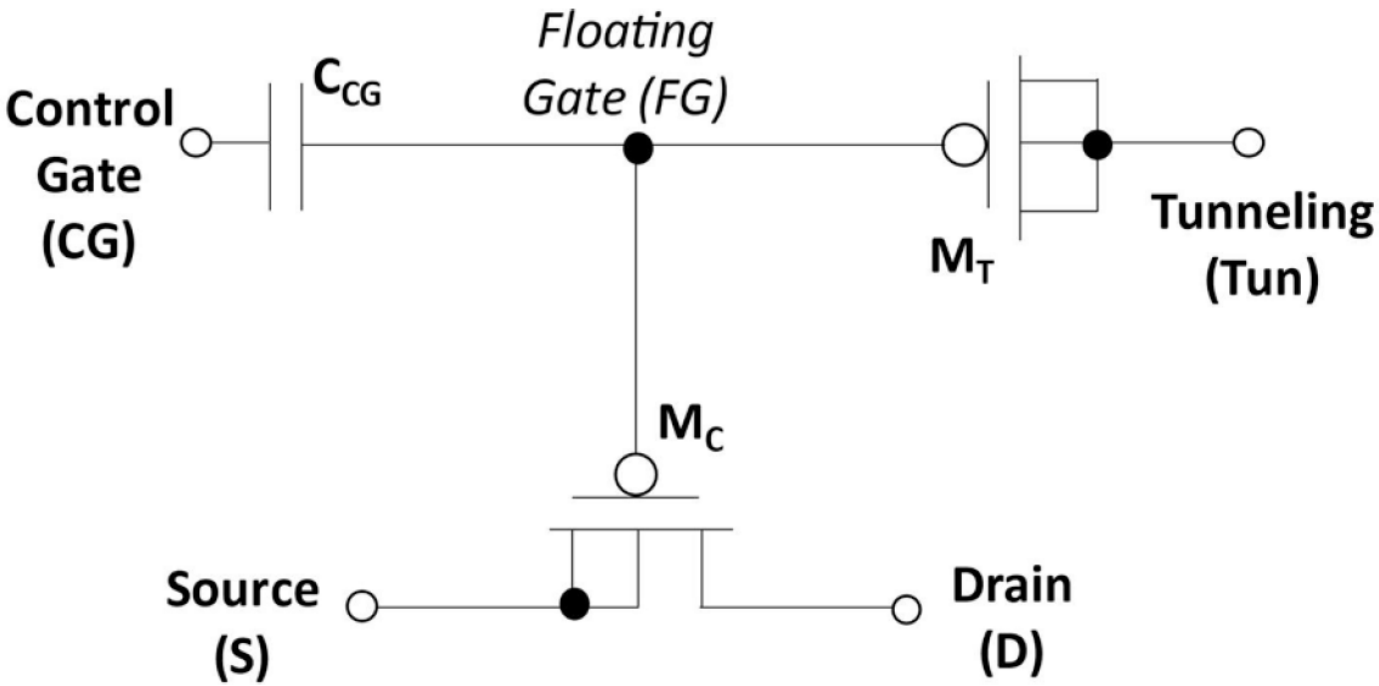




- It requires high voltages to enable tunneling (≈7V in our technology)

[M. Castriotta, Solid State Electronics 189 (2022)]

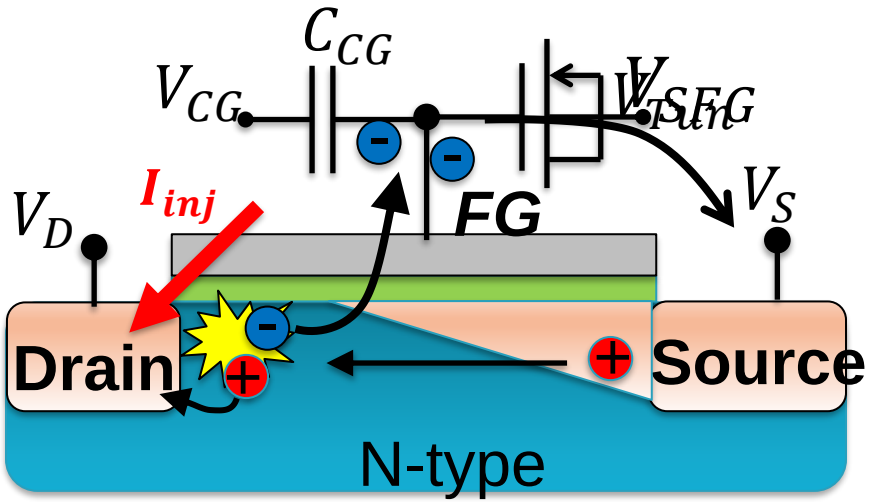
Floating gate in standard CMOS technology



- Hot electron injection using a p-type MOSFET
- The electrons are removed by tunneling (coarse global resetting of the floating gates)

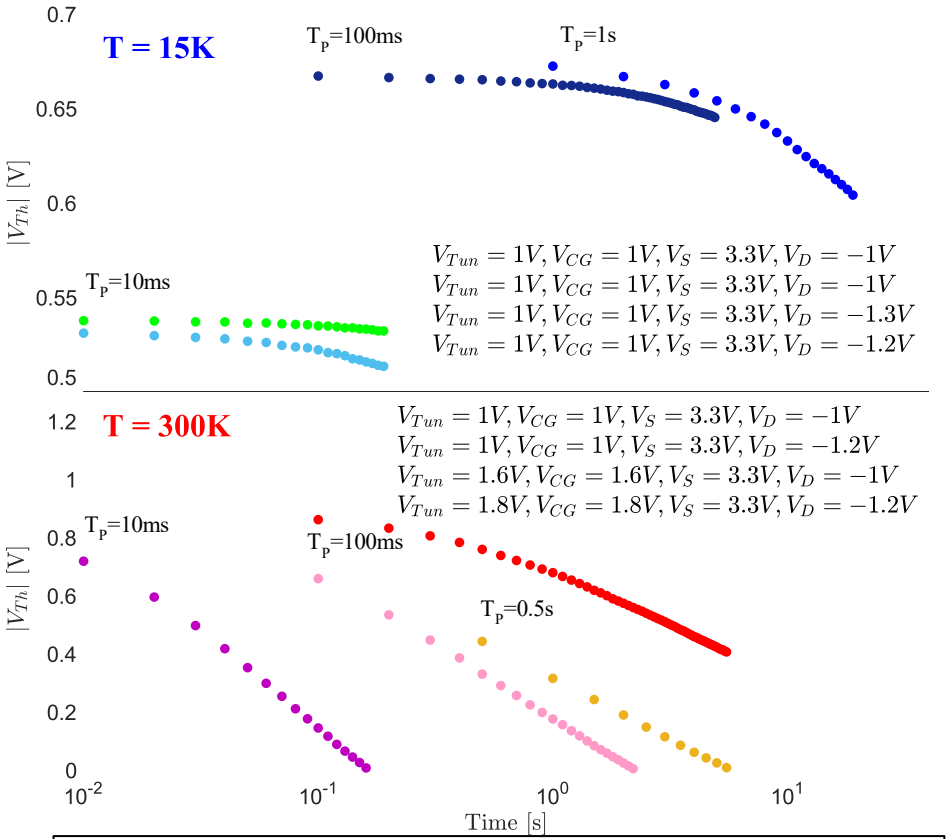
[M. Castriotta, Solid State Electronics 189 (2022)]

Hot electron injection in p-type FG transistor



holes collide with sufficient energy (≈ 3/2 E_{gap}) to liberate additional electron-hole pairs

- $V_{SFG}>|V_T|$ (ON)
- $V_{SD}>>0V$ (high electric field)
- $V_{SD}>>V_{SFG}$ ($V_{FG}>V_D$)

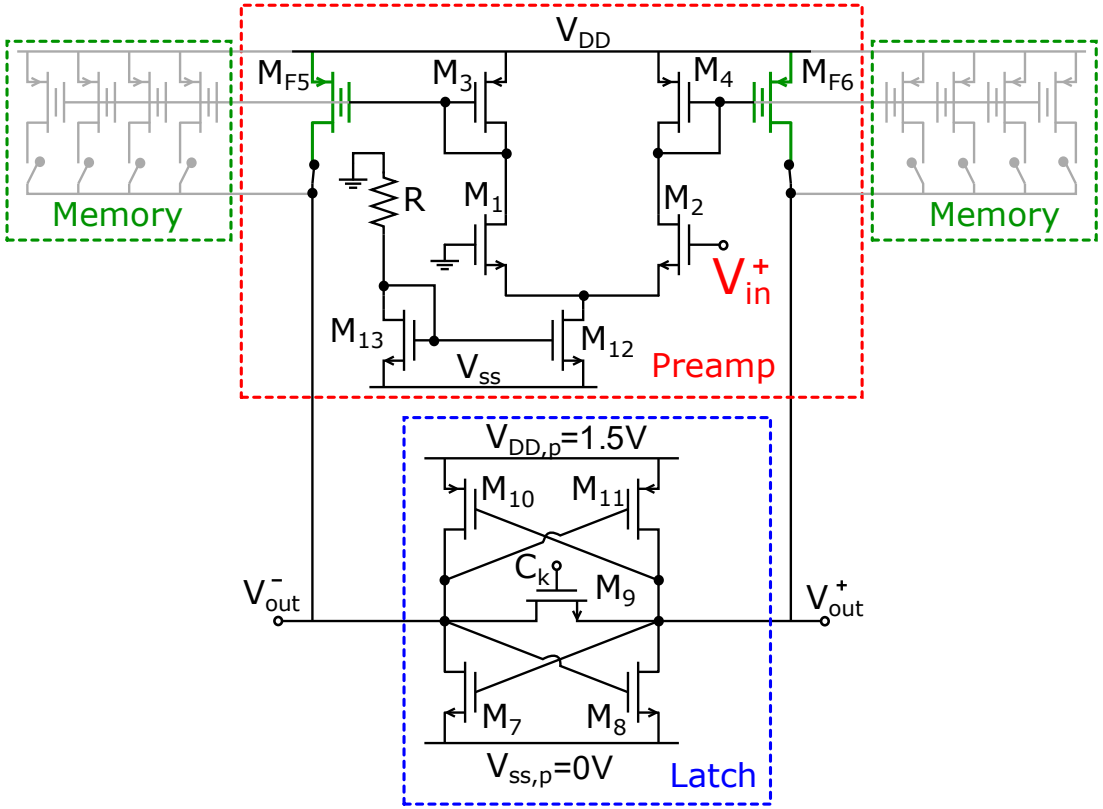


$$I_{inj} = C(V_{SD} - \gamma V_{ov})^3 I_d e^{-\frac{B}{V_{SD}-\gamma V_{ov}}}$$

[M. Castriotta, Solid State Electronics 189 (2022)]

Programmable comparator based on FGs

Standard 150-nm CMOS Technology

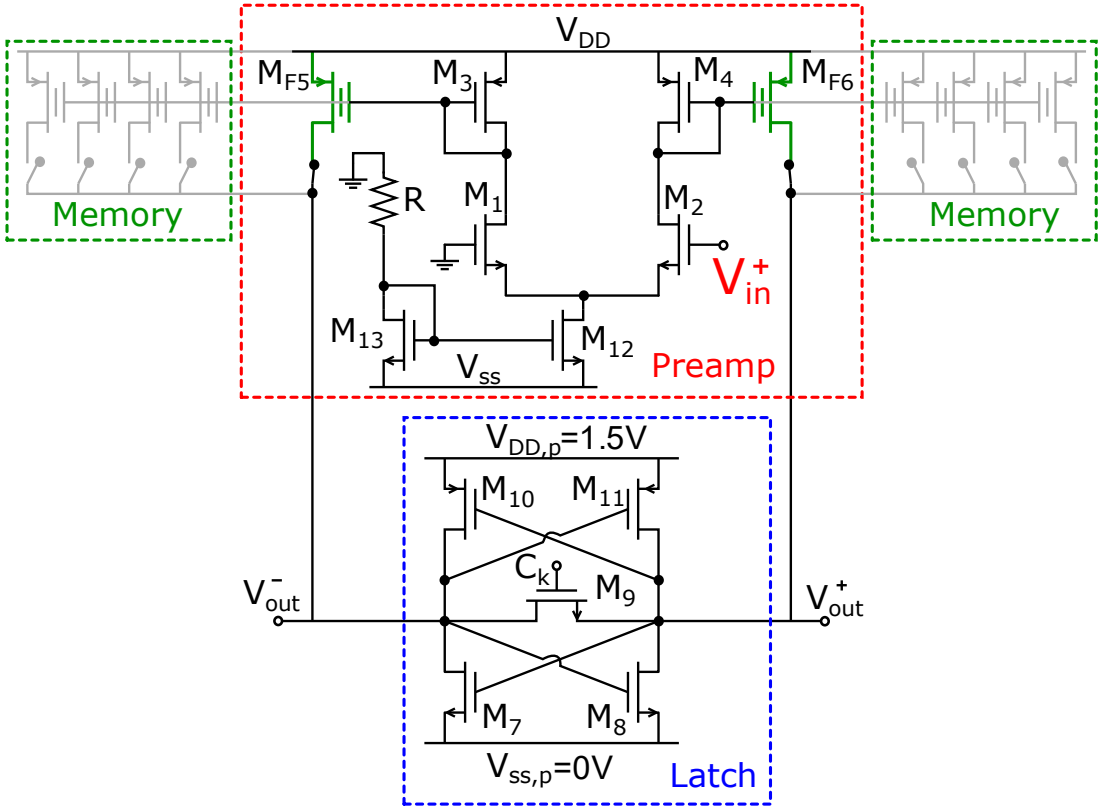


For standard latched comparator:

- $M_{F5}=M_{F6}=M_3=M_4$
- if $V_{in}>0V$ and C_k goes low:
  - $I_{F6}>I_{F5}$
  - V_{out+} ↗, V_{out-} ↘

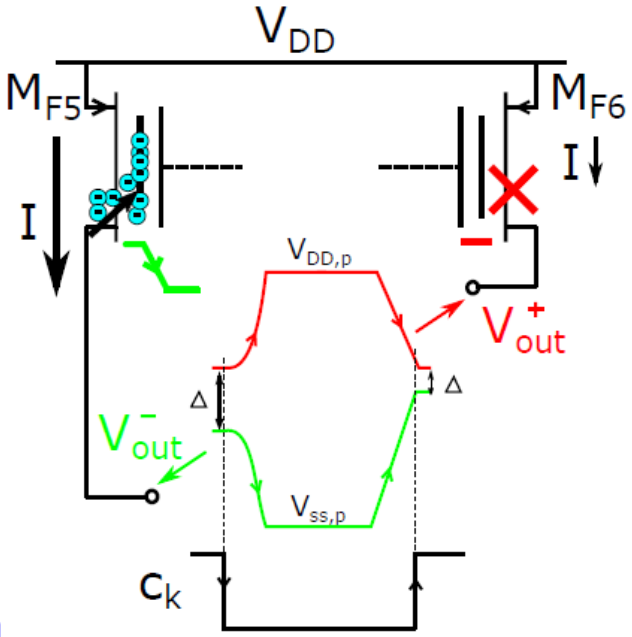
Programmable comparator based on FGs

Standard 150-nm CMOS Technology



❑ Programming phase:

- $V_{DD,p}, V_{ss,p}$ and C_k shift down by 2.3V
- Differential charge injection
- $|V_{th}|$ of M_{F5} decreases and its curent increases
- The comparator threshold is increased after each clock cycle

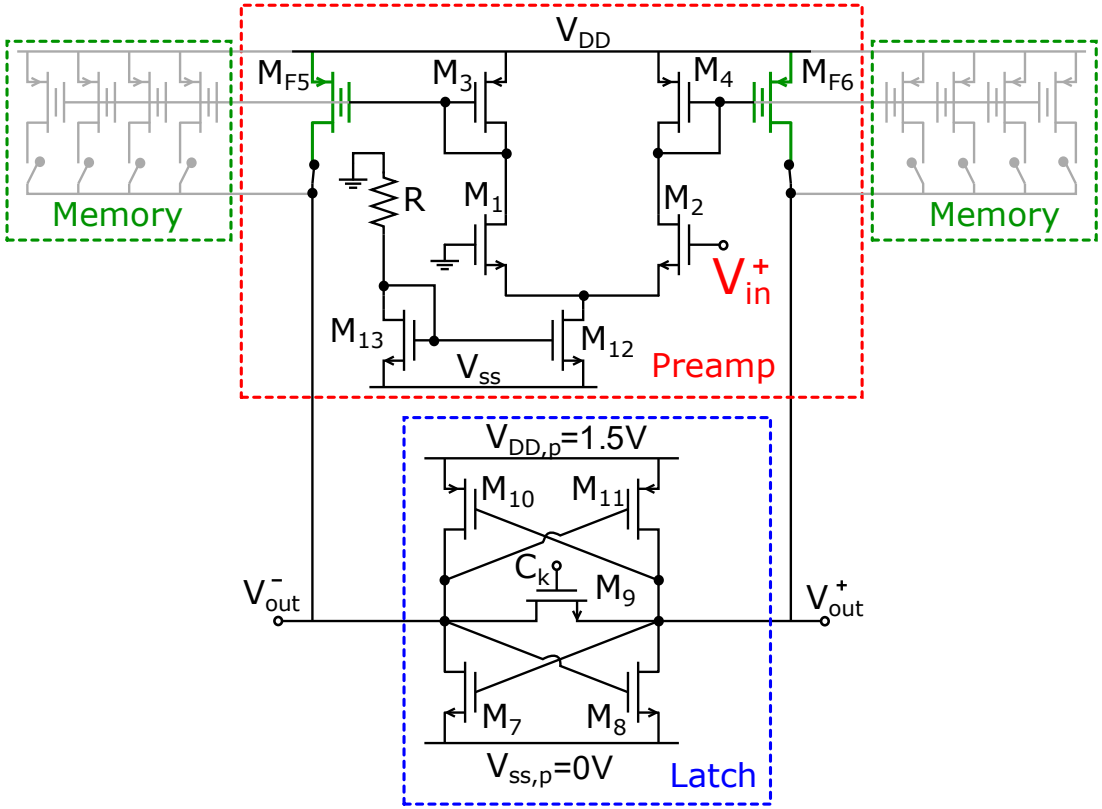


After tens of clock cycles, the threshold voltage of M_{F5} is such that $I_{F5} \approx I_{F6}$

→ the threshold voltage of the comparator is $\approx V_{in}$

Programmable comparator based on FGs

Standard 150-nm CMOS Technology



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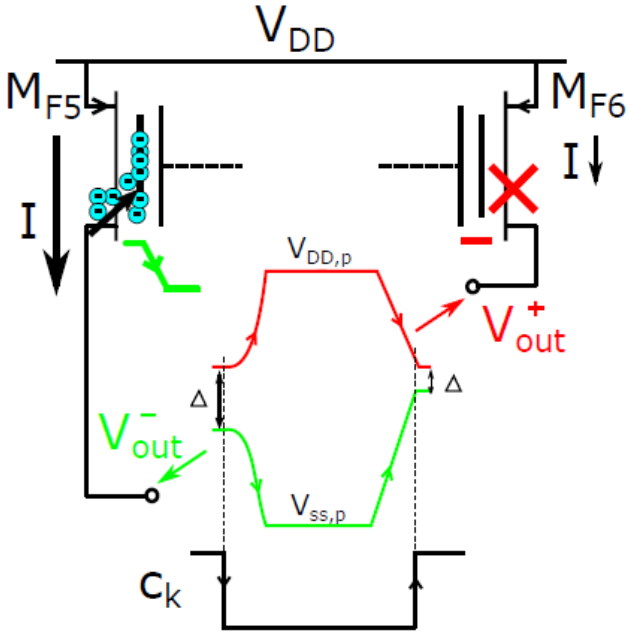
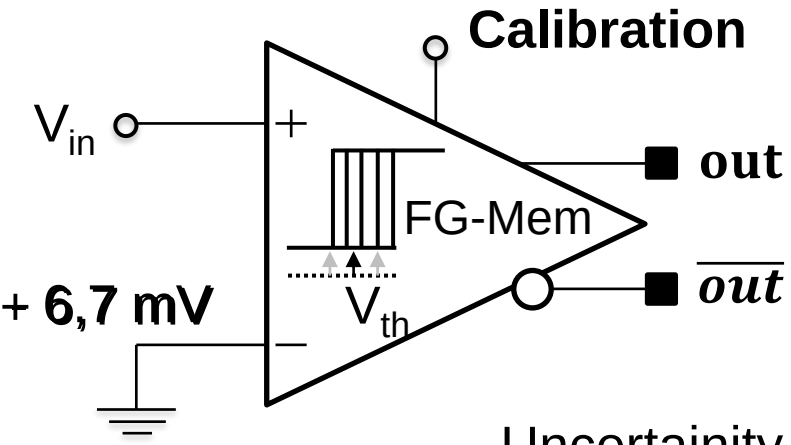


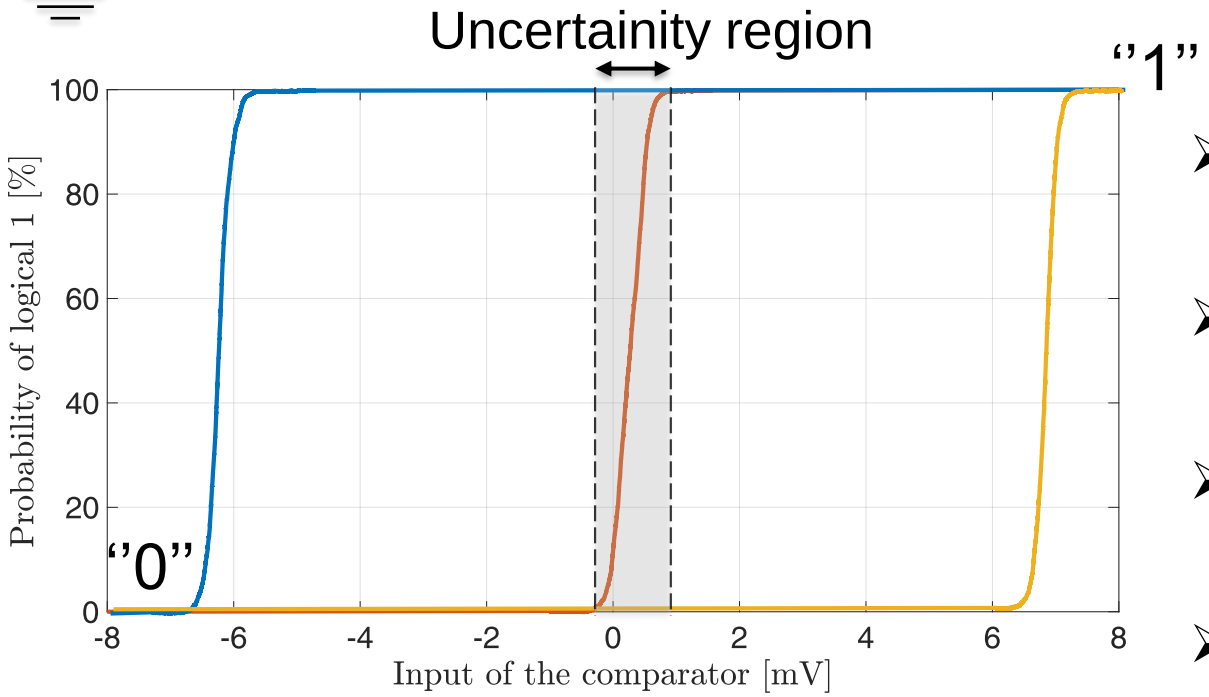
❑ Evaluation phase:

Standard latched comparator with threshold stored in a pair of FG-transistor M_{F5} and M_{F6}

Characterization of the FG comparator at 4,2 K

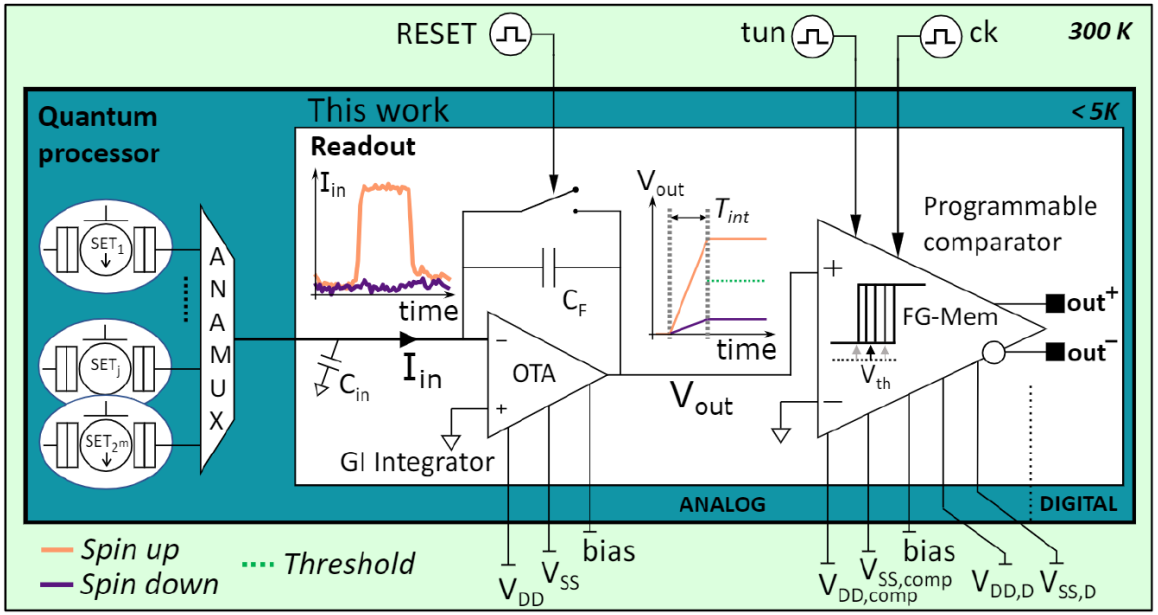


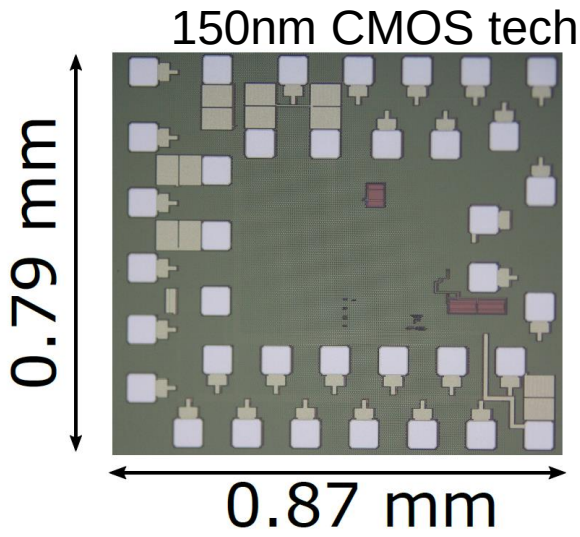
Programming accuracy: **300μV**
6 Sigma: **840 μV**
Calibration time**: 175 ms**
Fall/rise time**: 2 ns**



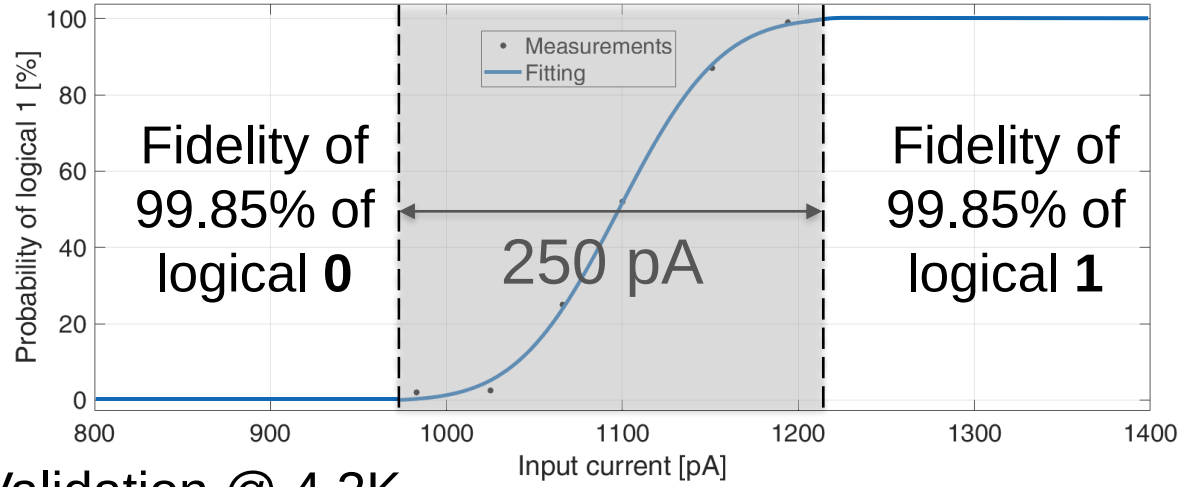
- Self-programmable threshold voltage
- Internal permanent FG memory
- "Zero" power dissipated by the memory
- Easy implementation of a TDM architecture

Characterization of the readout at 4.2 K





No off-chip components!

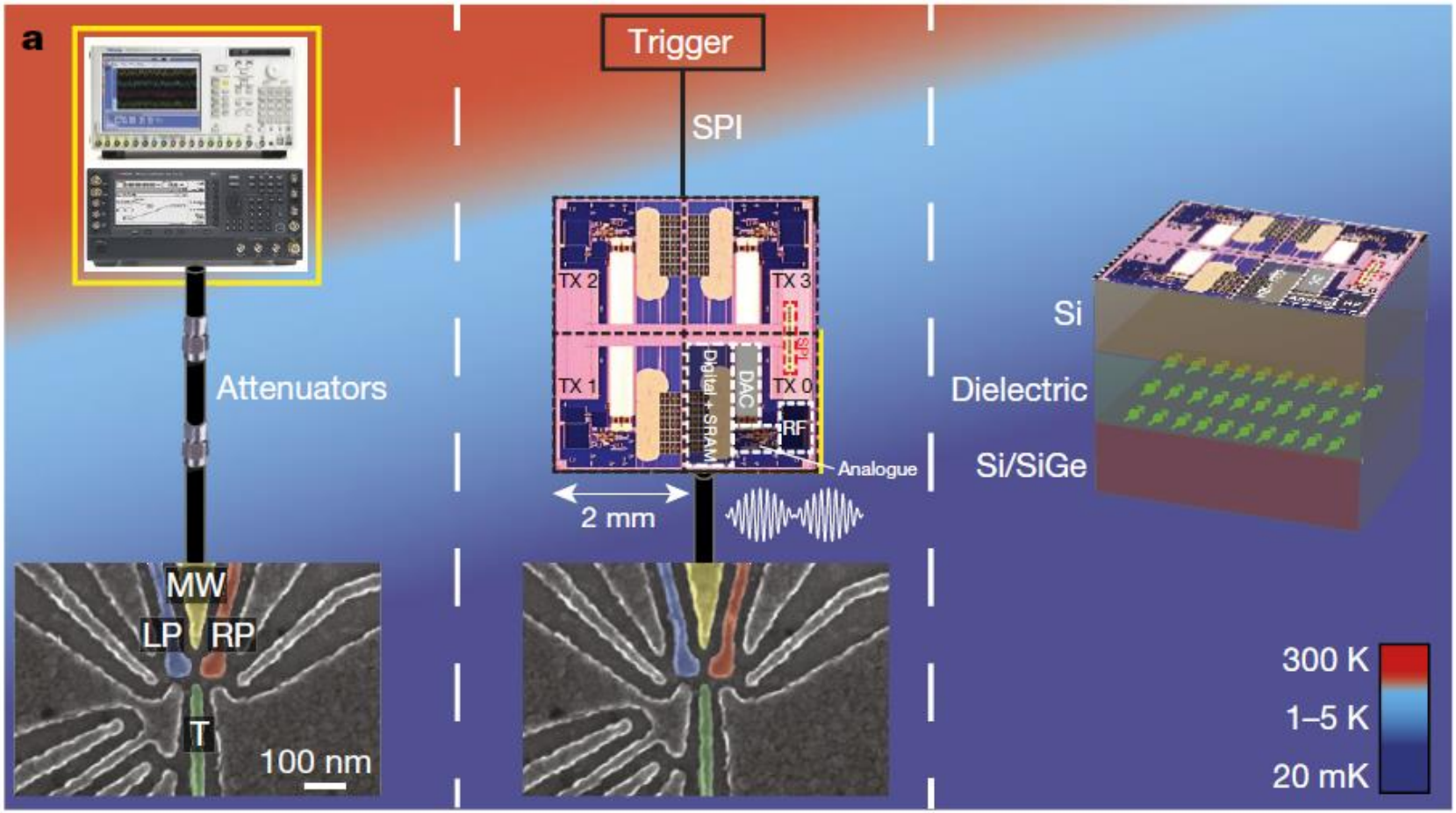


Validation @ 4.2K

Threshold current: **1.1 nA**
6 Sigma: **250 pA**
Readout time**: 500 ns**
Power consumption: **1.2 mW**

[M. CASTRIOTTA et al., IEEE *Solid-state circuits letters* (2023)]

Cryogenic quantum controllers



Today Tomorrow Future

X. Xue *et al.*, "CMOS-based cryogenic control of silicon quantum circuits," *Nature*, pp. 205–210, 2021

Cryogenic quantum controllers

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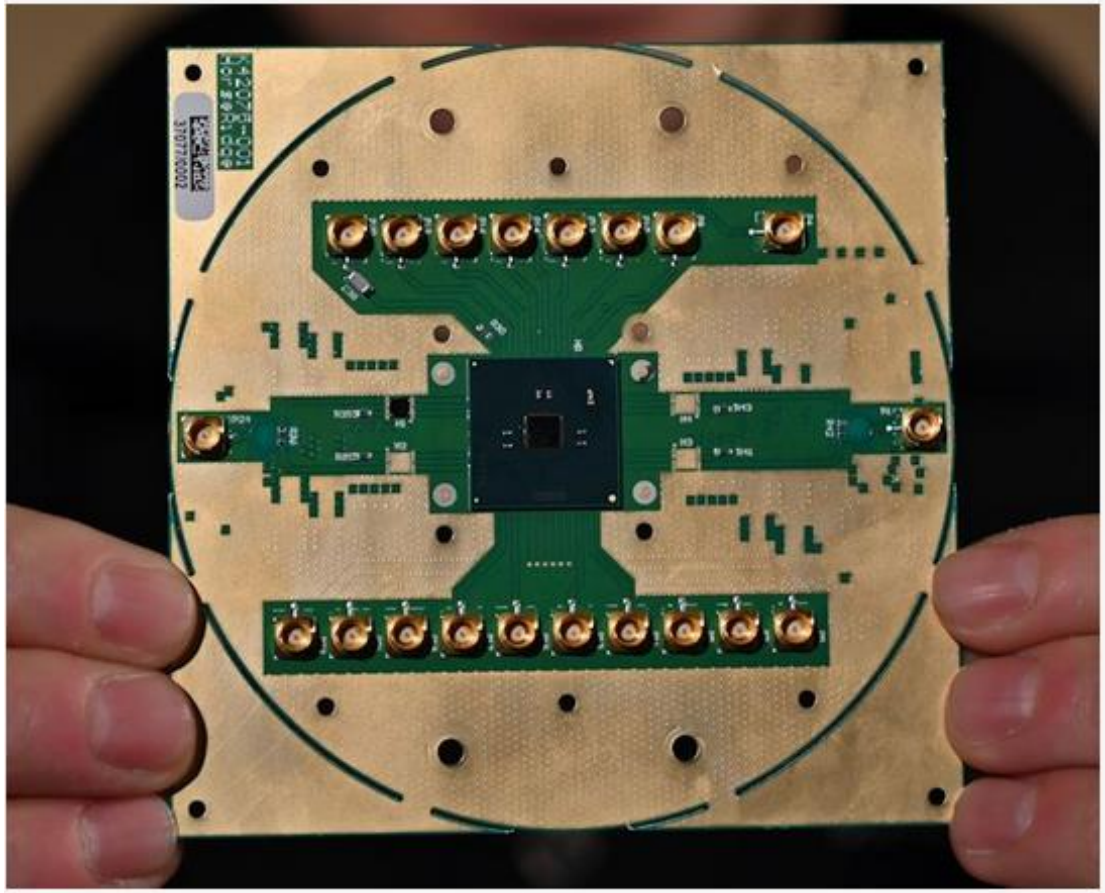
Intel Launches Horse Ridge Chip for Quantum Computing Systems

10 Comments

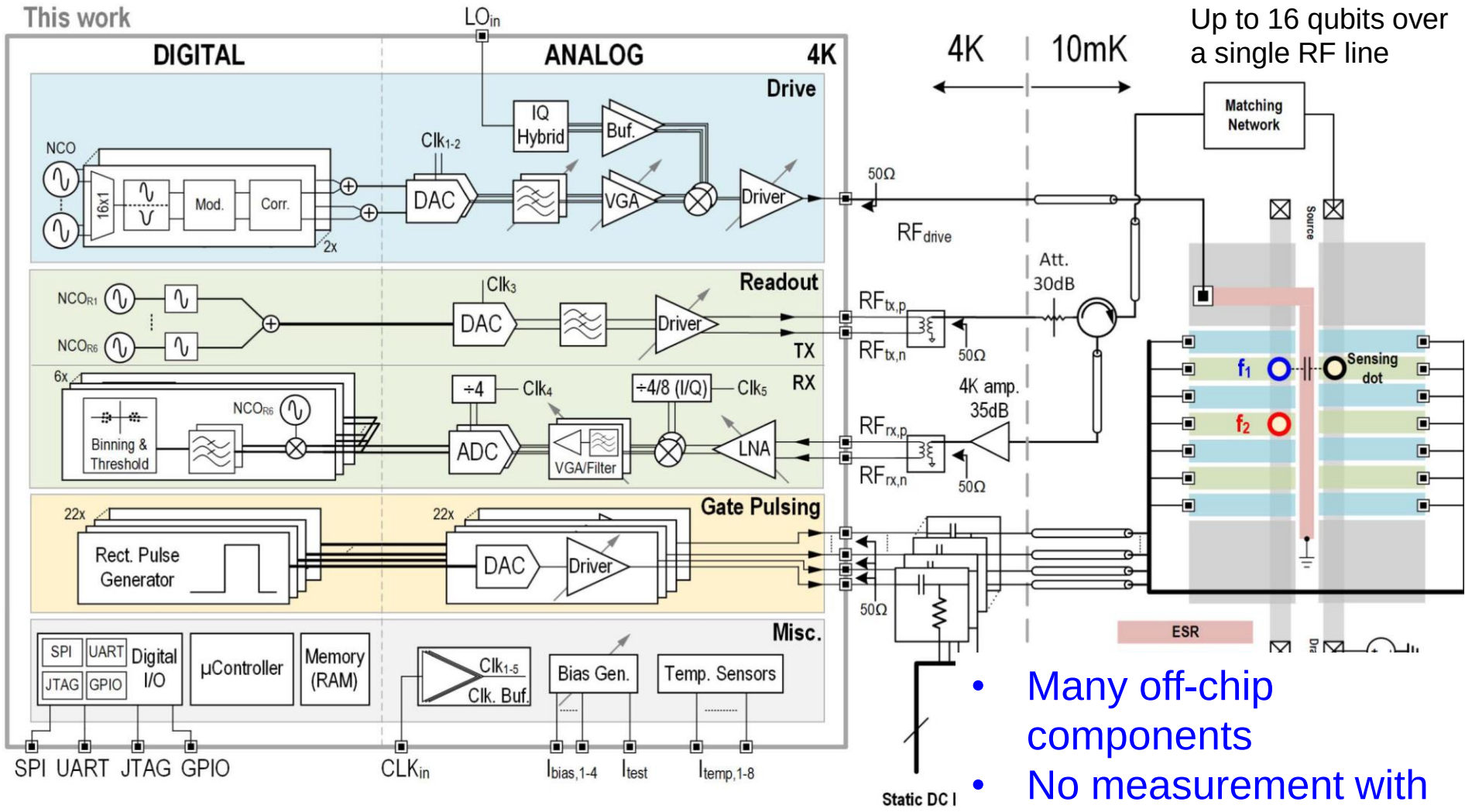
+ Add A Comment

by Anton Shilov on December 10, 2019 2:15 PM EST

Posted in Quantum Computing | Intel | Servers | Horse Ridge



Cryogenic quantum controller (spin q.) - Intel

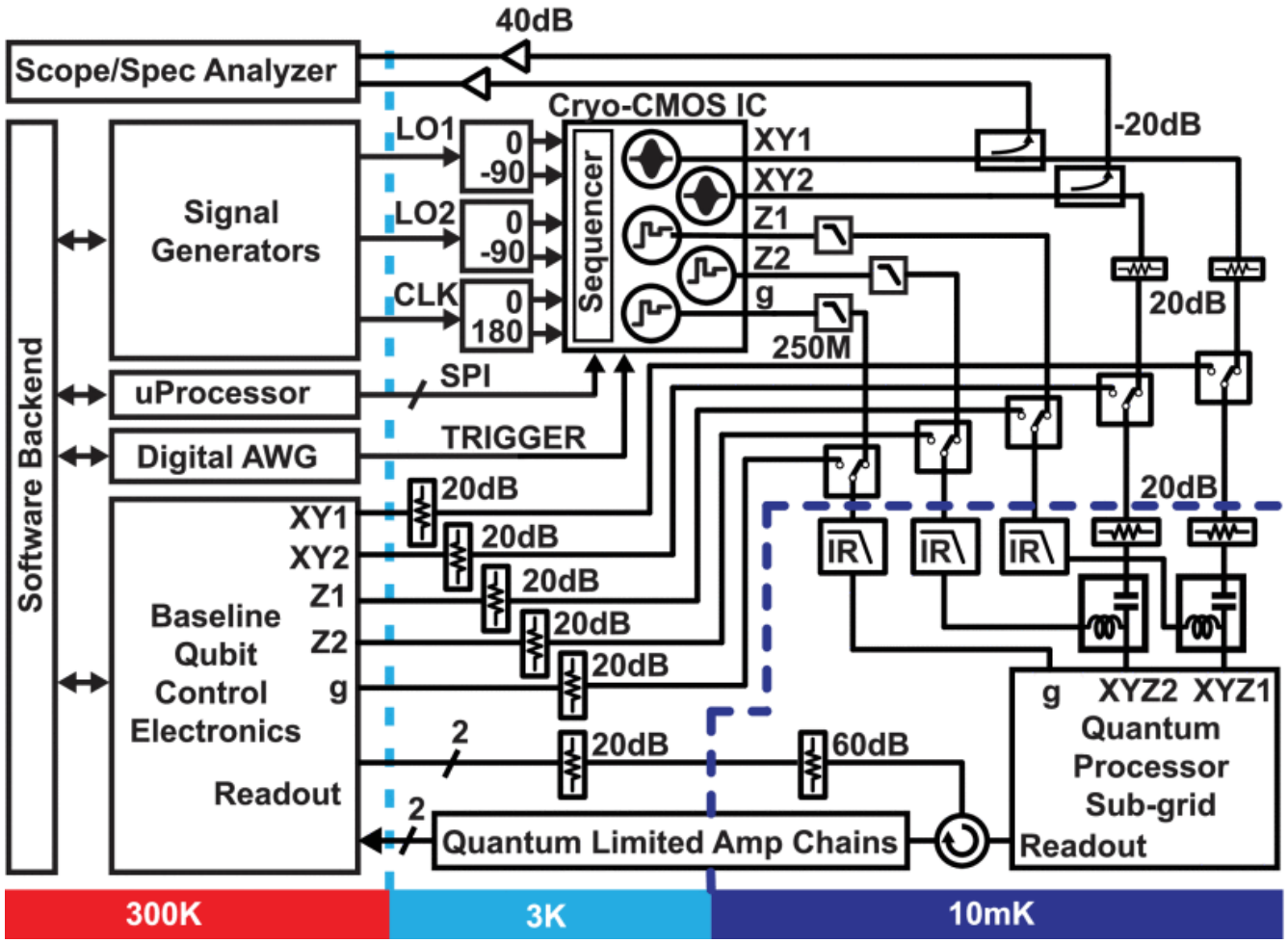


Up to 16 qubits over a single RF line

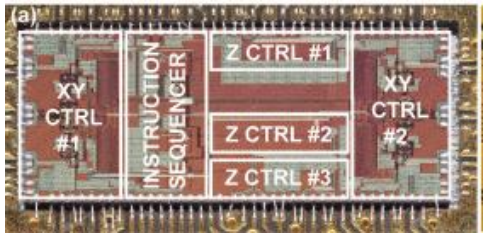
- Many off-chip components
- No measurement with real qubits

J. Park, et al. ,"A Fully Integrated Cryo-CMOS SoC for State Manipulatic
Pulsing of Spin Qubits," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3289–3306, 2021

Cryogenic quantum controller - Google



- superconducting qubits
- control of 2 qubits (measured!)
- 4mW/qubit
- RT readout
- 28 nm CMOS
- 1.8mm x 3.9mm



J. Yoo *et al.*, "Design and Characterization of a <4-mW/Qubit 28-nm Cryo-CMOS Integrated Circuit for Full Control of a Superconducting Quantum Processor Unit Cell," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 11, pp. 3044-3059, Nov. 2023,

Thank you for you attention!